WS01X-GA/GB Graphics Coprocessor

Maintenance Guide

EK-WS01X-MS-001

Digital Equipment Corporation
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About This Manual

Purpose of This Manual

This manual provides important WS01X-GA/GB graphics coprocessor configuration and testing information applicable to VAXstation 3100 Models 30, 38, 40, and 48 workstations. It also describes how to install and test the WS01X-GA/GB graphics coprocessor in a VAXstation 3100 Model 38.

Who Should Use This Manual

WS01X-GA/GB Graphics Coprocessor Installers

This manual is for anyone installing the WS01X-GA/GB graphics coprocessor in a VAXstation 3100 Model 38.

WS01X-GA/GB Graphics Coprocessor Maintainers

Anyone maintaining VAXstation 3100 Models 30, 38, 40, and 48 workstations with an installed WS01X-GA/GB graphics coprocessor will find important configuration and testing information in:

Section 1.1, Module Overview
Section 1.3, System Configuration
Section 2.12, Testing the System
Section 2.13, Resetting the Monitor Resolution Switch
Figure 2–11, WS01X-GA/GB Graphics Coprocessor Module
Table 2–1, Monitor Resolution Switch Settings
Chapter 3, Diagnostic Tests and Utilities

Structure of This Manual

This manual contains three chapters, an appendix, and an index.

- Chapter 1 describes significant differences and similarities between the WS01X-GA/GB graphics coprocessor and VS40X-PA graphics coprocessor. It also lists system configuration requirements.
- Chapter 2 tells you how to install and test the WS01X-GA/GB graphics coprocessor module.
- Chapter 3 tells you how to run diagnostic tests and test-pattern utilities.
- Appendix A lists part numbers for items in the WS01X-GA/GB graphics coprocessor installation kit.

1

Installation Prerequisites

This chapter tells you how to prepare to install the WS01X-GA/GB graphics coprocessor in a VAXstation 3100 Model 38 workstation.

1.1 Module Overview

The WS01X-GA/GB graphics coprocessor is for use with high- and low-resolution color monitors, and provides significantly higher performance than the VS40X-PA graphics coprocessor. The two coprocessors are plug compatible. In other words, the modules are physically the same size and use the same connectors in the workstation.

The WS01X-GA/GB graphics coprocessor operates with monitors having a display area of either 1280 × 1024 pixels (high resolution) or 1024 × 864 pixels (low resolution). The module's operation is set to match the monitor's resolution with the monitor resolution switch, a unique feature of the WS01X-GA/GB graphics coprocessor.

1.2 Installation Kit

The WS01X-GA/GB graphics coprocessor kit includes:

WS01X-GA/GB Graphics Coprocessor Owner's Manual
WS01X-GA/GB graphics coprocessor module
Module mounting hardware
Cross-tip screwdriver
Monitor video cable
Monitor coaxial cable filters (for VR290 monitors)
SPX label

In addition to the installation kit:

- You need a straight-tip screwdriver.

- When adding devices inside the system unit, take precautions to protect the system devices from static discharge. It is recommended that you wear a static wrist strap and place a static mat under the system unit.

1.3 System Configuration

The WS01X-GA/GB graphics coprocessor operating system and monitor configuration requirements are specified in Sections 1.3.1 through 1.3.3.

1.3.1 Operating System

The workstation's operating system must be VMS version 5.3-1 or higher. These versions include the correct release of DECwindows windowing system software.

The WS01X-GA/GB graphics coprocessor is not supported by the ULTRIX operating system or the VWS Workstation windowing system.

1.3.2 Monitor

The workstation must use the appropriate monitor. The following monitors are supported:

VRT19
VR150
VR160
VR260
VR262
VR290 (requires coaxial cable filters)
VR297
VR299

1.3.3 Monitor Video Cable

The appropriate monitor video cable is supplied with the WS01X-GA/GB graphics coprocessor module. Configurations using any other video cable are not supported.

2

Module Installation

This chapter describes the procedures for installing the WS01X-GA/GB graphics coprocessor in a VAXstation 3100 Model 38.

2.1 Preparing the System

To prepare the system unit:

1 Back up files stored on the system disk unit(s).

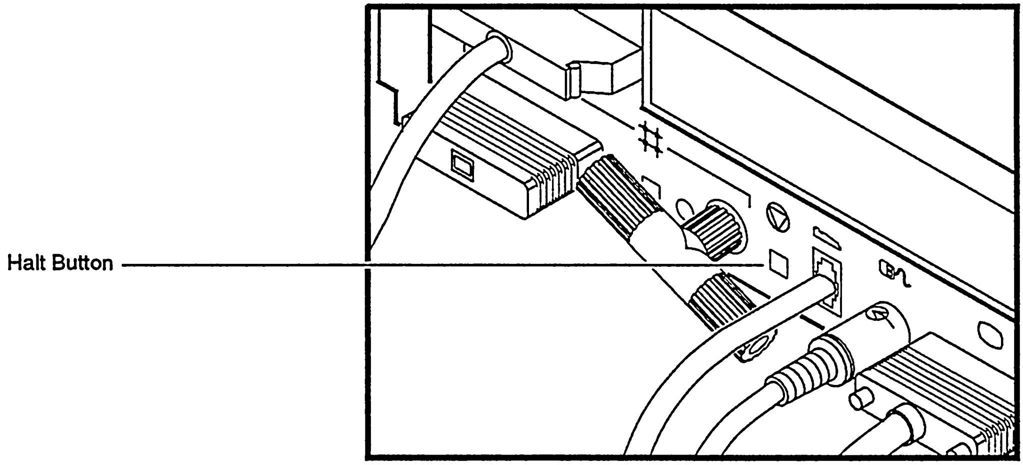
2 Perform an orderly system shut down. At the system prompt, enter:

```
$ @SYS$SYSTEM:SHUTDOWN
```

3 Put the system into console mode by pressing the halt button (Figure 2–1). In response to the console mode prompt, enter:

```
>>> SET HALT 3 [Return]
```

Figure 2–1 System Halt Button



MLO-002330

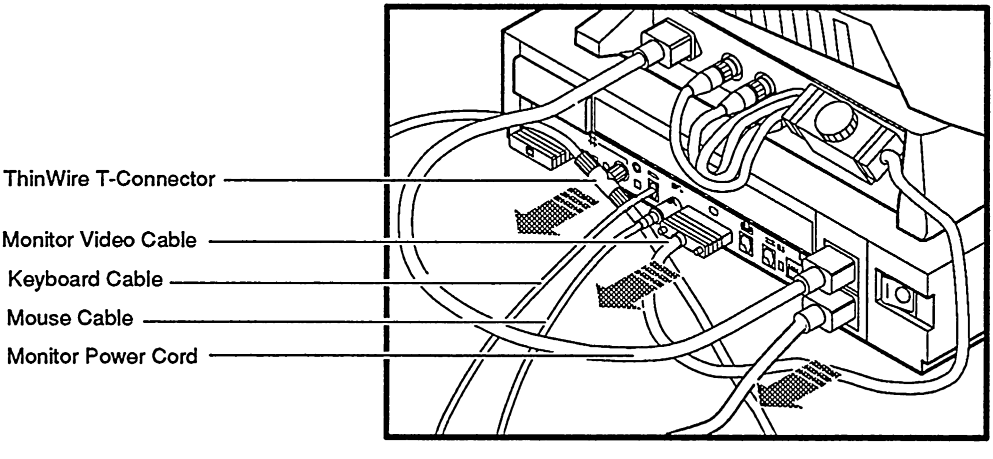
The next time the system is turned on it will halt at the console prompt. You can then use the diagnostic tests to verify the installation.

4 Display current system configuration using the SHOW DEVICE and TEST 50 console commands. Make a copy of the current configuration to compare with the configuration after the module is installed (Section 2.12).

5 Turn off the system unit.

6 Disconnect the following cords (Figure 2–2) before you remove the system unit cover. The cords can be disconnected in any order.

Figure 2–2 System Unit and Monitor Rear Connector Panels and Cables



- Disconnect the monitor power cord.
- Disconnect the keyboard cable.
- Disconnect the mouse cable.
- Disconnect the monitor video cable from the system unit. Loosen the thumbscrews and remove the cable from the system unit.
- The correct monitor video cable is supplied with the WS01X-GA/GB graphics coprocessor installation kit, and will be installed later (Section 2.9). Follow the directions in the monitor guide to disconnect the cable from the monitor.
- Disconnect the ThinWire T-connector. Loosen the center leg of the T-connector and remove it from the system unit. You do not have to remove terminators or cables connected to the T-connector.

Warning *The monitor is heavy and you may need another person's help to lift it.*

7 Remove the monitor from the top of the system unit and set it aside.

8 Take precautions to protect the system devices from static discharge.

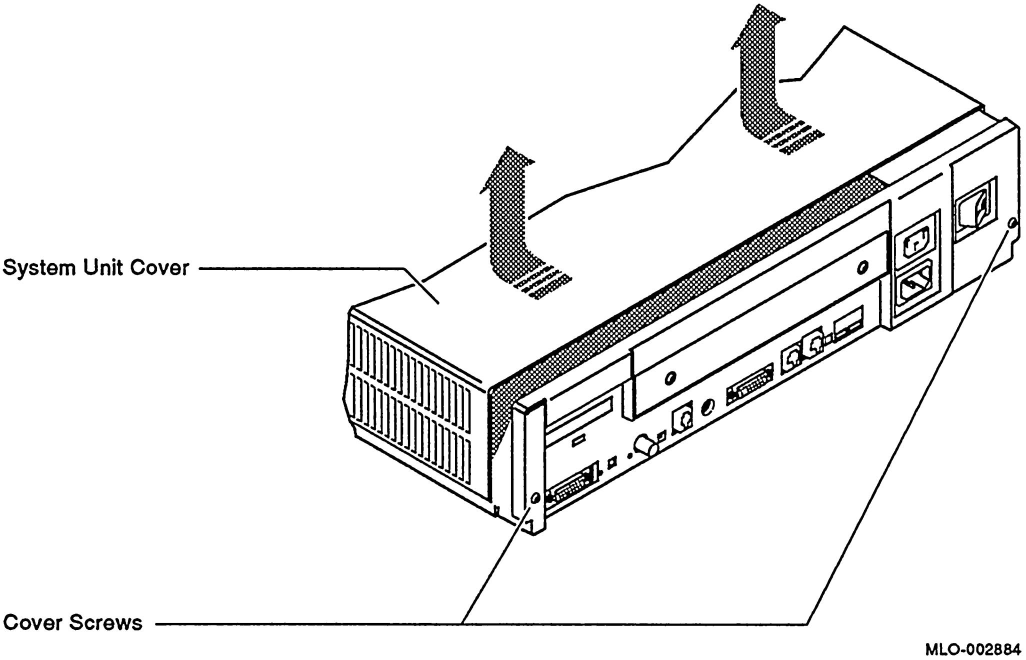
Caution *When adding devices inside the system unit, it is recommended that you wear a static wrist strap and place a static mat under the system unit.*

9 Remove the system unit cover as follows:

Warning *As with any electrical system, it is a fire hazard to turn on system power with the cover removed.*

- Loosen, but do not remove, the two captive cross-head screws at the outside edges of the system unit rear connector panel (Figure 2–3).

Figure 2–3 Removing the System Unit Cover (Rear View)

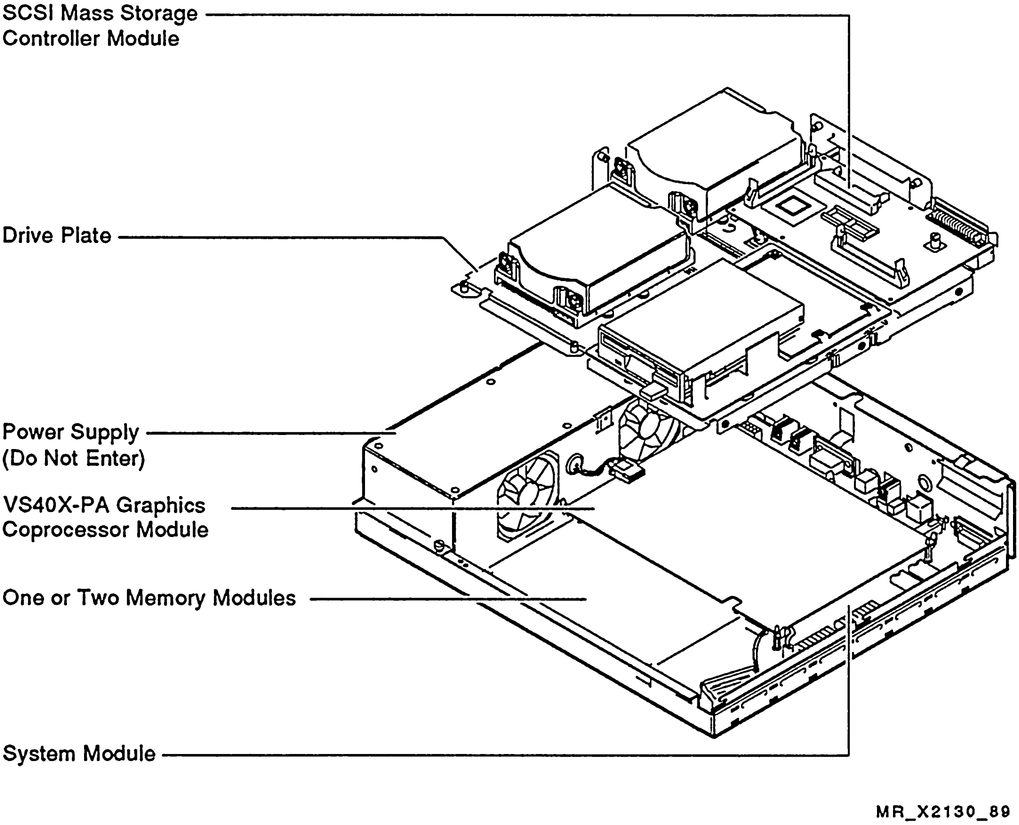


- Slide the system unit cover toward the front of the system unit, then lift it up and away from the system unit.

Warning *Do not attempt to enter the power supply shown in Figure 2–4. Dangerous voltages are present inside the power supply and it has no serviceable parts.*

10 Continue at Section 2.2.

Figure 2–4 Device and Module Locations


SCSI Mass Storage Controller Module
Drive Plate
Power Supply (Do Not Enter)
VS40X-PA Graphics Coprocessor Module
One or Two Memory Modules
System Module
MR_X2130_89

2.2 Removing the Drive Plate

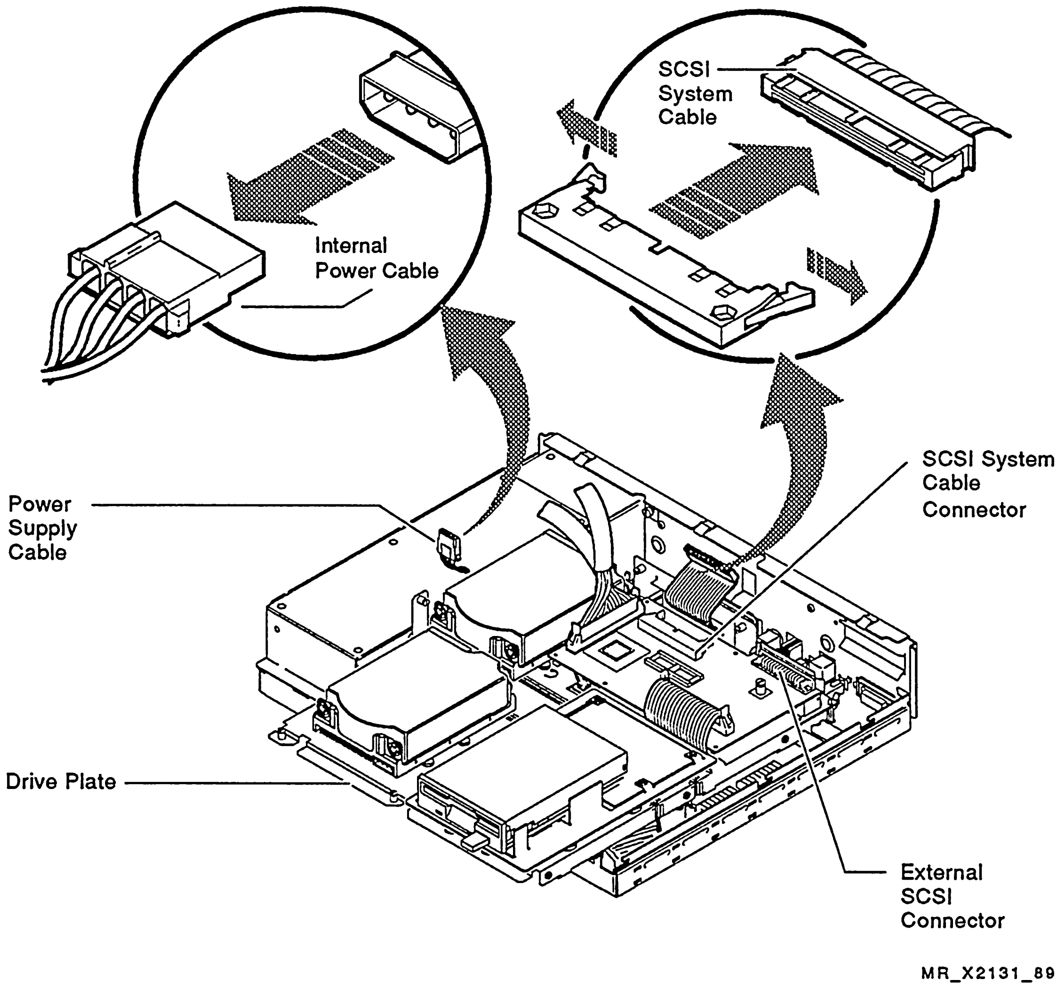
If the system does not have a drive plate, skip this section and continue at Section 2.3.

You do not have to remove devices mounted on the drive plate in order to remove it from the system unit. To remove the drive plate:

1 Disconnect the power supply cable (Figure 2–5).

2 Disconnect either the terminator or cable from external SCSI connector on the SCSI mass storage controller module.

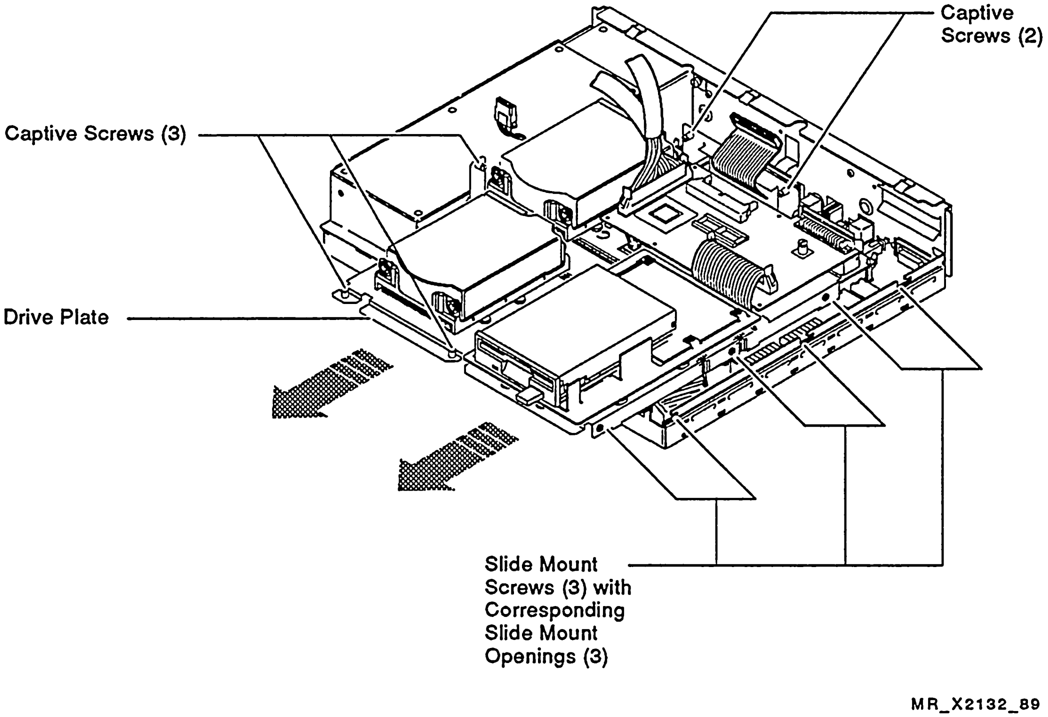
Figure 2–5 Disconnecting Drive Plate Cables



3 Disconnect the SCSI system cable from the mass storage controller by opening the latches on the sides of the connector.

4. See Figure 2–6. Loosen, but do not remove, the eight drive plate mounting screws: five captive slot-head screws and three slide-mount cross-head screws.

Figure 2–6 Removing the Drive Plate


Captive Screws (2)
Captive Screws (3)
Drive Plate
Slide Mount Screws (3) with Corresponding Slide Mount Openings (3)
MR_X2132_89

5. Slide the drive plate assembly forward and lift it out of the system unit. Set it aside.
6. Continue at Section 2.3.

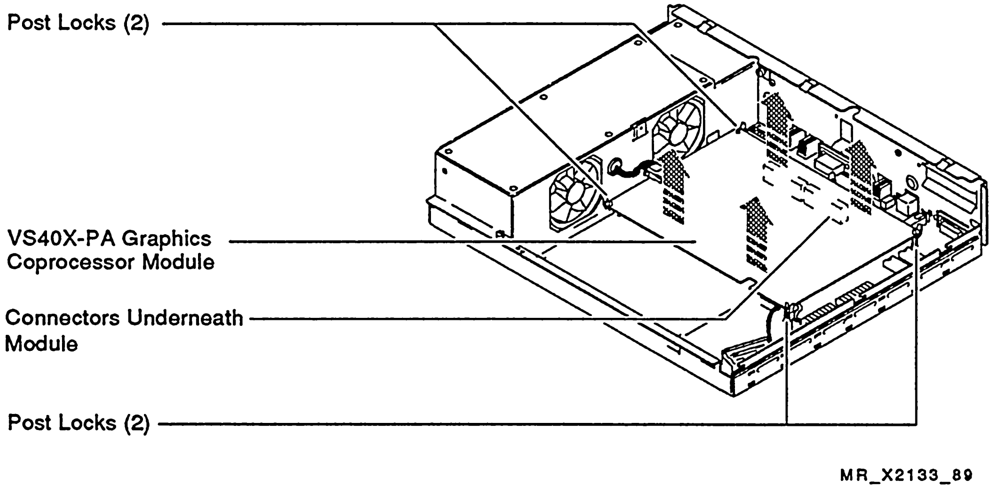
2.3 Removing a VS40X-PA Graphics Coprocessor

If the system does not have a VS40X-PA graphics coprocessor, skip this section and continue at Section 2.4.

Figure 2–7 shows you how to remove a VS40X-PA graphics coprocessor. Proceed as follows:

Caution *Always handle modules by their edges to avoid physical and static discharge damage.*

Figure 2–7 Removing a VS40X-PA Graphics Coprocessor


Post Locks (2)
VS40X-PA Graphics Coprocessor Module
Connectors Underneath Module
Post Locks (2)
MR_X2133_89

1. Lift the corners of the module as far as necessary to free it from the four post locks, and lift it out of the system unit. The connectors underneath the module disconnect as the module is lifted. Set the module aside.
2. Continue at Section 2.4.

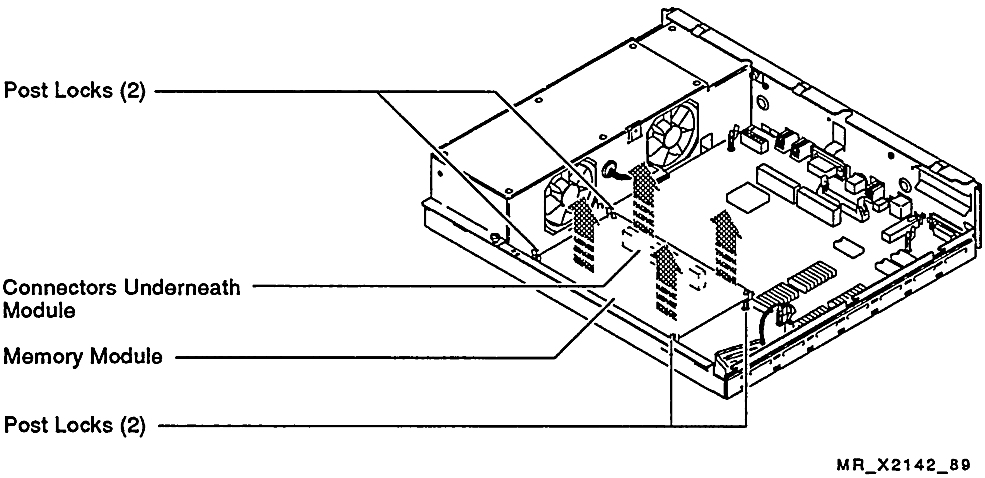
2.4 Removing Memory Option Modules

If the system has no memory option modules, skip this section and continue at Section 2.5.

Figure 2–8 shows you how to remove a one-module memory option. The procedure is the same for a two-module memory option as the modules are physically and electrically connected together. Proceed as follows:

Caution *Always handle modules by their edges to avoid physical and static discharge damage.*

Figure 2–8 Removing a Memory Option Module



1 Lift the corners of the module as far as necessary to free it from the four post locks and lift it out of the system unit. The connectors underneath the module disconnect as the module is lifted. Set the module aside.

2 Continue at Section 2.5.

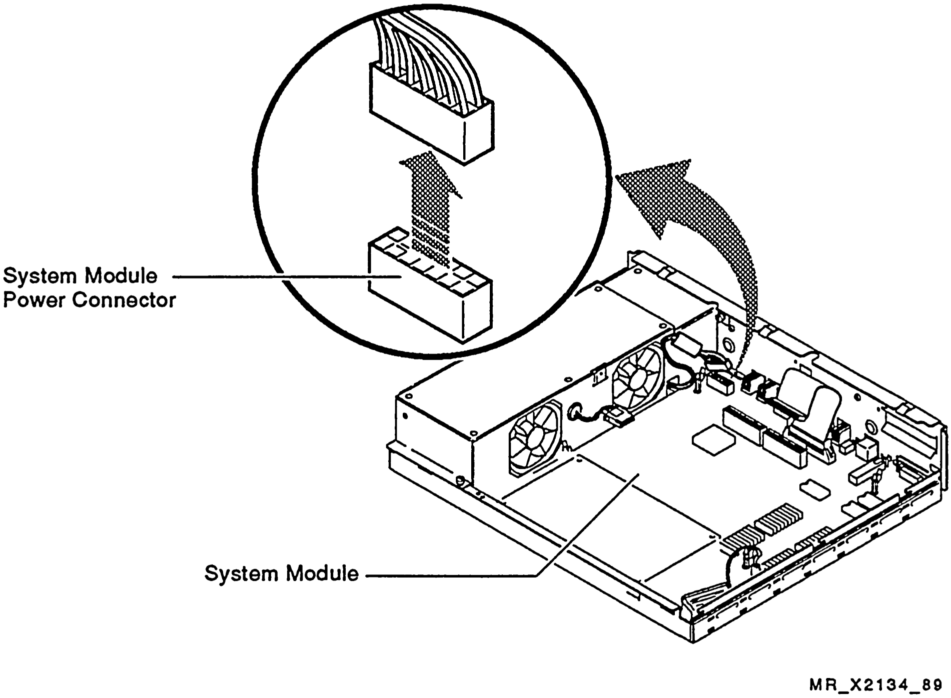
2.5 Installing the Mounting Hardware

The WS01X-GA/GB graphics coprocessor mounting hardware consists of three mounting brackets and three cross-tip screws for installing the brackets. An identifying letter, A, B, or C, is stamped into each bracket.

To install the mounting hardware:

1 Disconnect the power cable from the system module (Figure 2–9). To free the connector, press the tab on its side.

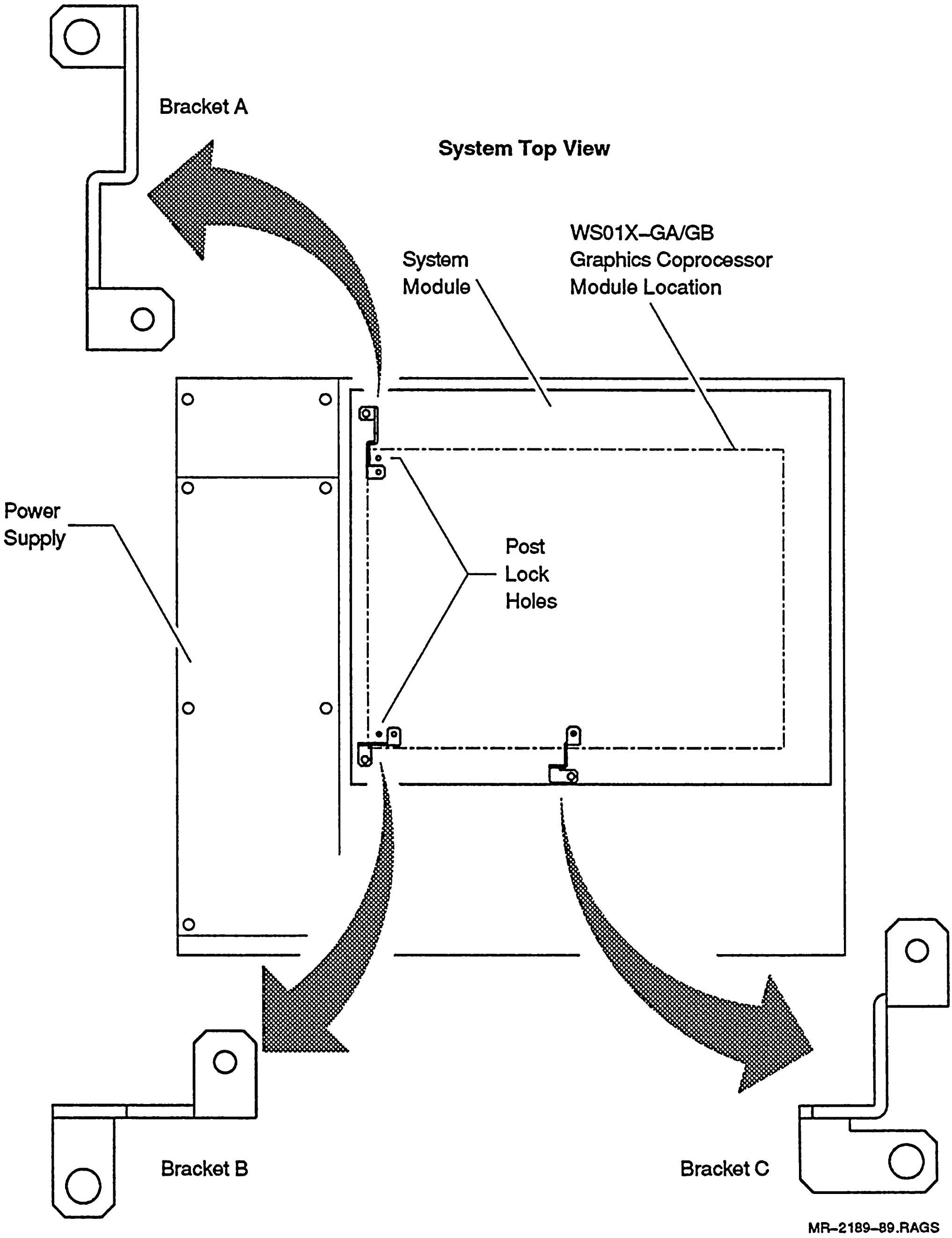
Figure 2–9 Removing the System Module Power Cable



2 Figure 2–10 is a top view of the system unit. It shows the location of the brackets and screws. Install the brackets as follows:

- **Bracket A:** At the rear corner of the system module next to the power supply, remove the cross-tip screw. Place the screw through the unthreaded hole in bracket A, and loosely refasten the screw and bracket to the system module.

Figure 2–10 WS01X-GA/GB Graphics Coprocessor Mounting Bracket Locations



- **Bracket B:** At the front corner of the system module next to the power supply, remove the cross-tip screw. Place the screw through the unthreaded hole in bracket B, and loosely refasten the screw and bracket to the system module.
- **Bracket C:** At the center of the front edge of the system module, remove the cross-tip screw. Place the screw through the unthreaded hole in bracket C, and loosely refasten the screw and bracket to the system module.

The bracket mounting screws will be tightened when the WS01X-GA/GB graphics coprocessor is installed.

3 Continue at Section 2.6.

2.6 Installing the WS01X-GA/GB Graphics Coprocessor

Caution *When handling the WS01X-GA/GB graphics coprocessor, grasp the module at the center of its front and rear edges.* ***Do not*** *press on the wire leads for the Timing Buffer Chip underneath the module (Figure 2–11).*

Before installing the module, set its monitor resolution switch to match the resolution of the workstation's monitor. Table 2–1 lists the switch settings for supported monitors. As Figure 2–11 shows, the monitor resolution switch is switch number 2 in a two-switch package. (Switch number 1 is inactive and can be in either position.)

Table 2–1 Monitor Resolution Switch Settings

Monitor Type	Resolution	Switch 2	Switch 1[1]
VRT19	1280 x 1024[2]	ON	–
VR150	1024 x 864	OFF	–
VR160	1024 x 864	OFF	–
VR260	1024 x 864	OFF	–
VR262	1024 x 864	OFF	–

---

[1] Switch 1 is inactive and can be in either position.

[2] VRT19 resolution switch on LOW (66 Hz). This switch is located on the rear panel of the VRT19 monitor.

(continued on next page)

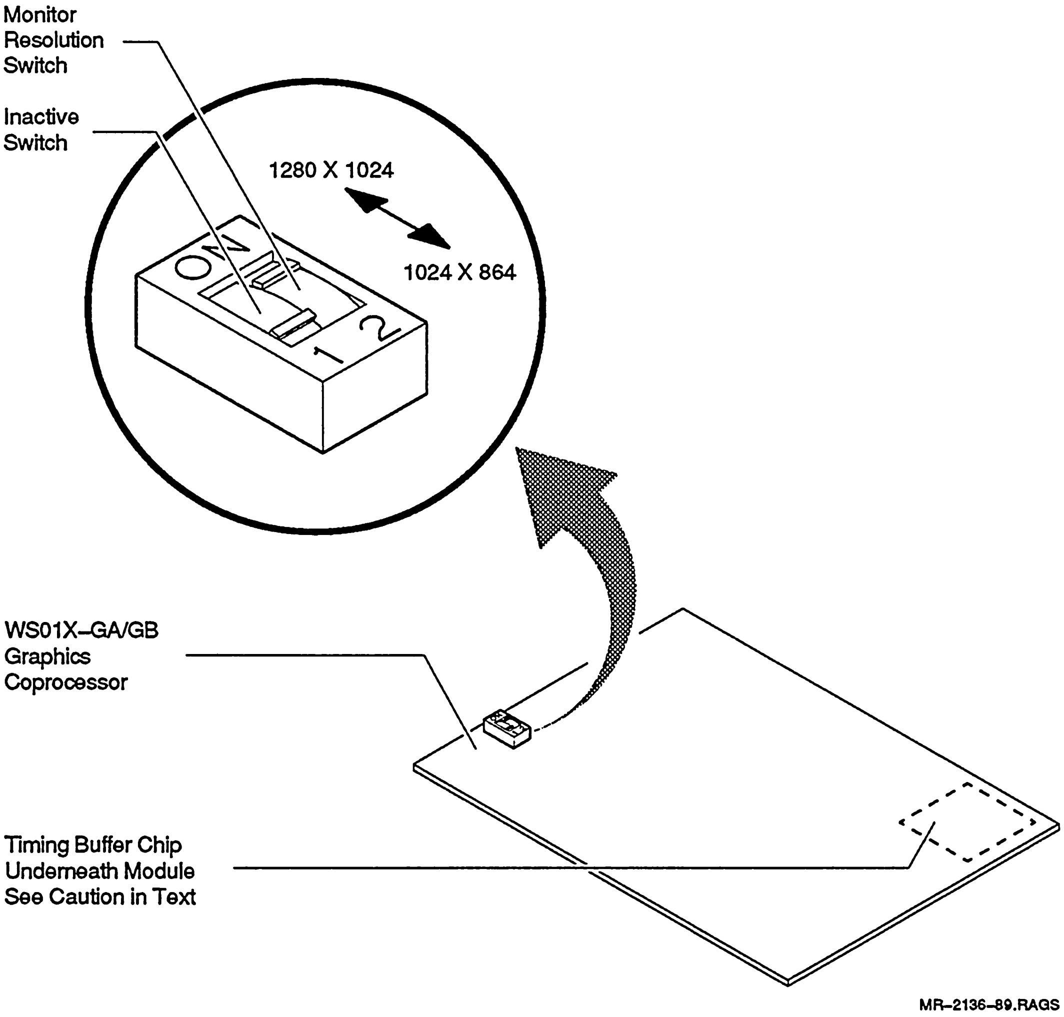
Table 2–1 (Cont.) Monitor Resolution Switch Settings

Monitor Type	Resolution	Switch 2	Switch 1[1]
VR290[3]	1024 x 864	OFF	–
VR297	1024 x 864	OFF	–
VR299	1024 x 864	OFF	–

[1] Switch 1 is inactive and can be in either position.

[3] The VR290 requires the use of coaxial cable filters.

Figure 2–11 WS01X-GA/GB Graphics Coprocessor Module


Monitor Resolution Switch
Inactive Switch
1280 X 1024
1024 X 864
WS01X–GA/GB Graphics Coprocessor
Timing Buffer Chip Underneath Module See Caution in Text
MR–2136–89.RAGS

Set the switch, if necessary, and install the module as follows:

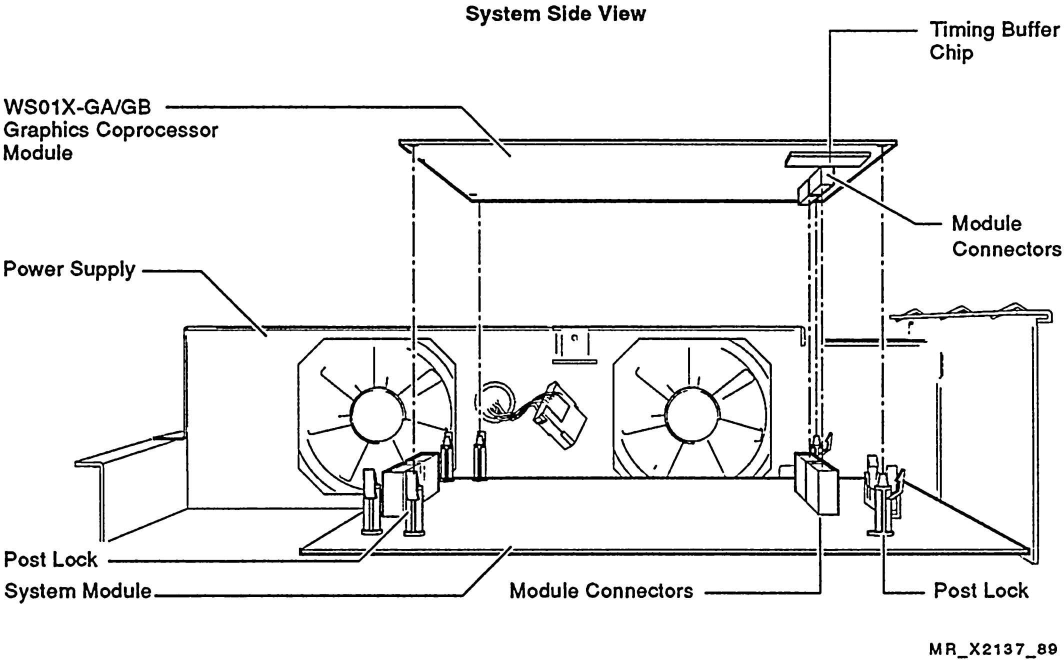
Caution *Do not use a graphite-lead pencil to set the switch.*

1. If the switch is covered with transparent tape, remove the tape (it need not be reinstalled). Use a ballpoint pen or similar object to move the monitor resolution switch to the correct position.

Note *You can change the position of the monitor resolution switch after the WS01X-GA / GB graphics coprocessor is installed. See Section 2.13.*

2 Grasp the module at the center of its front and rear edges, and position it over the four post locks and two connectors on the system module (Figure 2–12). Note that the post-lock holes are nearest to the corners of the module. Do not press on the wire leads for the Timing Buffer Chip.

Figure 2–12 Graphics Coprocessor Connectors and Post Locks



3 Press down on the graphics coprocessor module until it locks onto the four post locks. For a good connection, press down firmly on the graphics coprocessor module above the connectors to the system module.

4 The graphics coprocessor module is mounted on top of mounting brackets A, B, and C. Fasten the module to the mounting brackets, as follows:

- **Bracket A:** Align the threaded hole in bracket A with the mounting hole at the rear corner of the module next to the power supply (Figure 2–10). Note that a post-lock hole is nearest to the corner of the module and the bracket mounting hole is next to it. Loosely fasten the module to the bracket with a cross-tip screw.

- **Bracket B:** Align the threaded hole in bracket B with the mounting hole at the front corner of the module next to the power supply. Note that a post-lock hole is nearest to the corner of the module and the bracket mounting hole is next to it. Loosely fasten the module to the bracket with a cross-tip screw.
- **Bracket C:** Align the threaded hole in bracket C with the hole at the center of the front edge of the module. Loosely fasten the module to the bracket with a cross-tip screw.

5 Tighten both screws in each mounting bracket.

6 Reconnect the power cable to the system module.

7 Continue at Section 2.7.

2.7 Replacing Memory Option Modules

If you do not have to replace any memory option modules, continue at Section 2.8.

To replace a memory option module:

CAUTION *Always handle modules by their edges to avoid physical and static discharge damage.*

1 Position the memory module over the four post locks and two connectors on the system module. Two post locks are on the system module and two are on the system unit.

Figure 2–13 shows you how a one-module memory option is joined to the system module and Figure 2–14 shows you how a two-module memory option is joined to the system module.

Figure 2–13 One-Module Memory Option Connectors

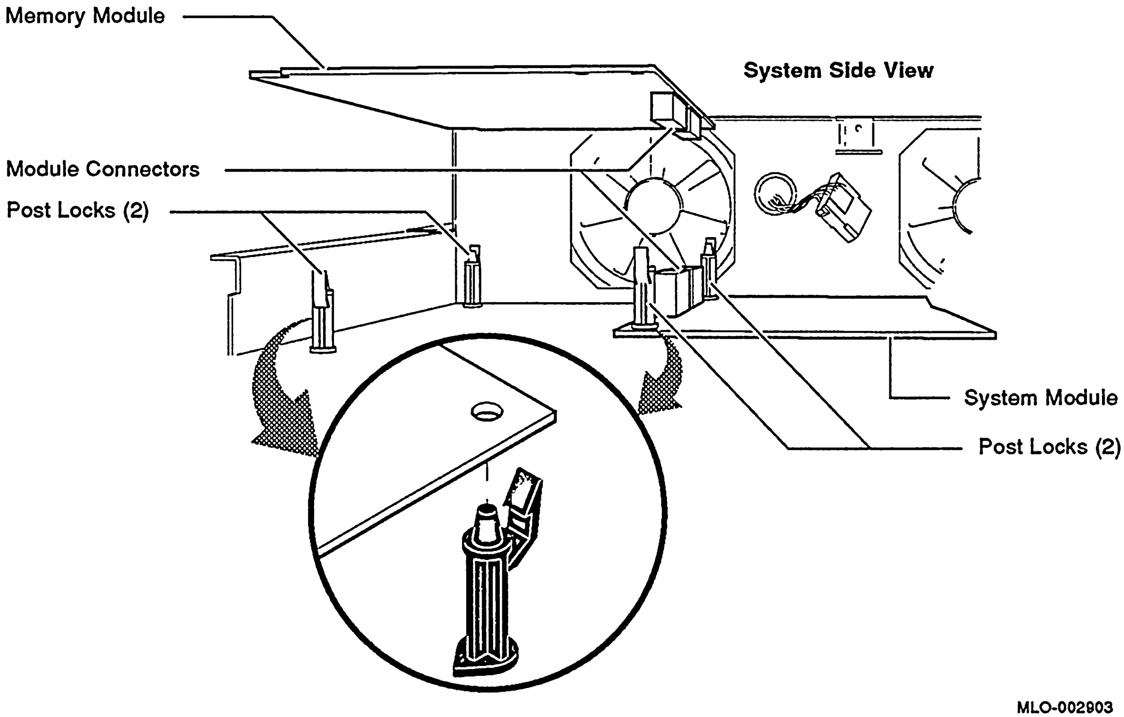
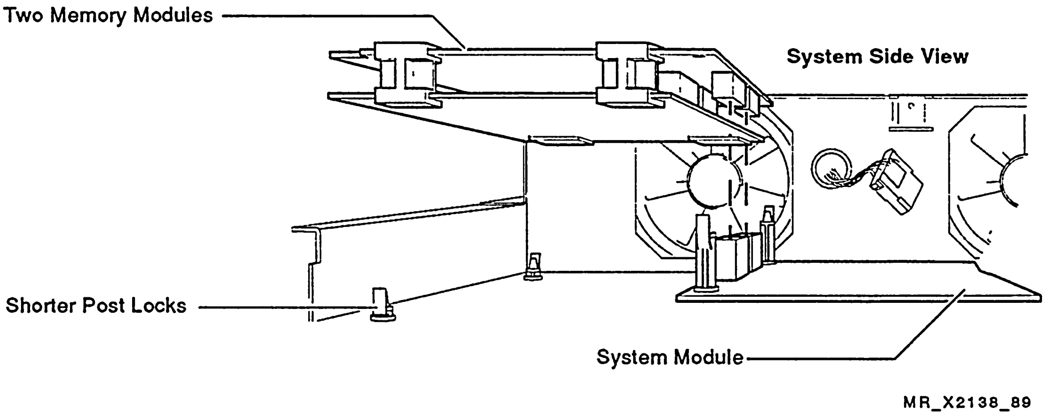
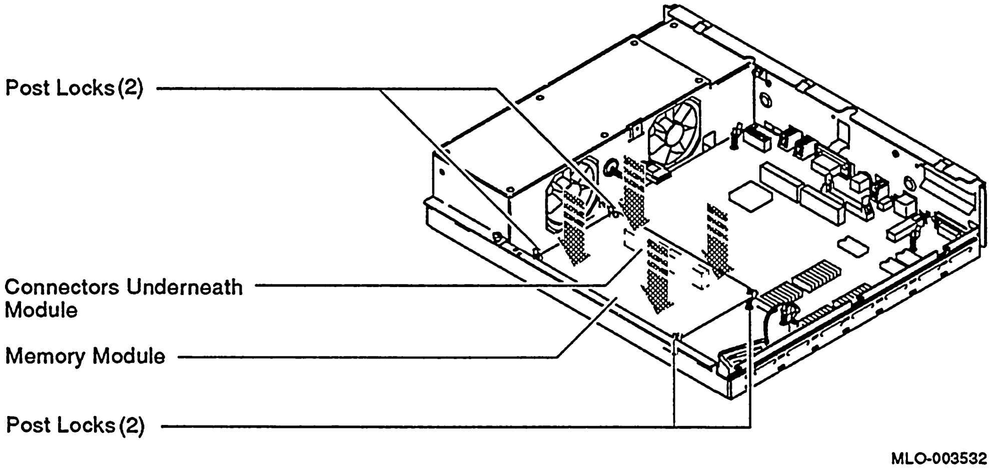


Figure 2–14 Two-Module Memory Option Connectors



2 Press down on the memory module until it locks onto the four post locks. For a good connection, press down firmly on the memory module above the connectors to the system module. Figure 2–15 shows a one-module memory option. The procedure is essentially the same for two-module memory options.

Figure 2–15 Replacing Memory Option Modules



3 Continue at Section 2.8.

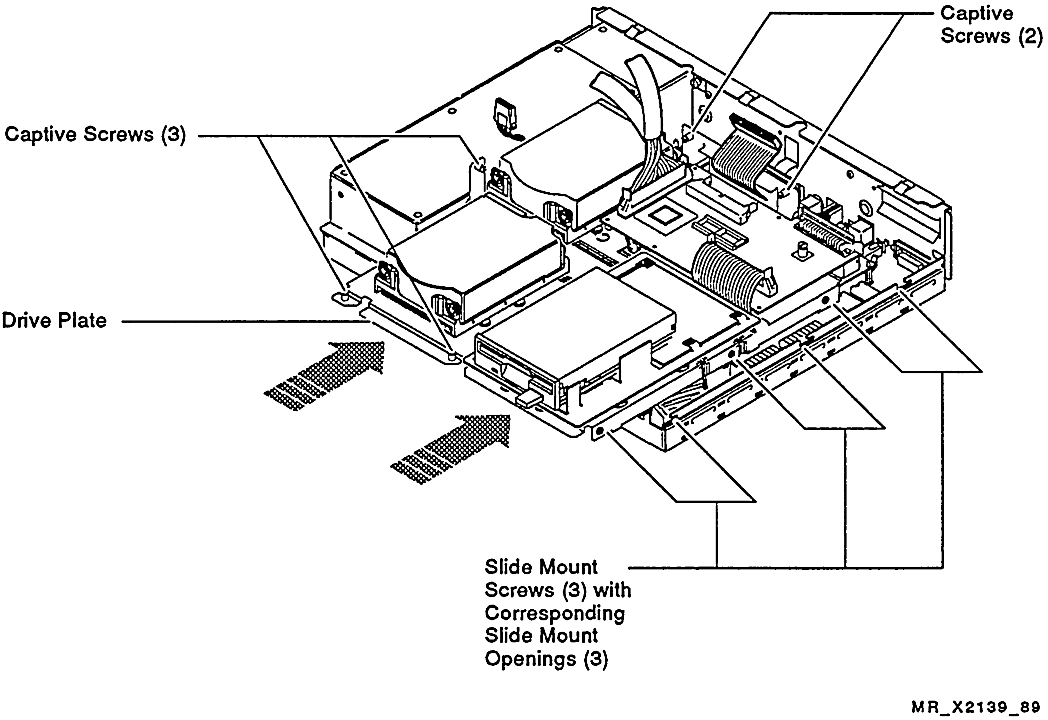
2.8 Replacing the Drive Plate

If you do not have to replace a drive plate, continue at Section 2.9.

To replace a drive plate:

1 Align the slide mount openings on the right side of the drive plate with the three slide mount screws, and slide the drive plate towards the rear of the system unit (Figure 2–16). Make sure the SCSI system cable goes through the drive plate handle (Figure 2–17).

Figure 2–16 Replacing the Drive Plate

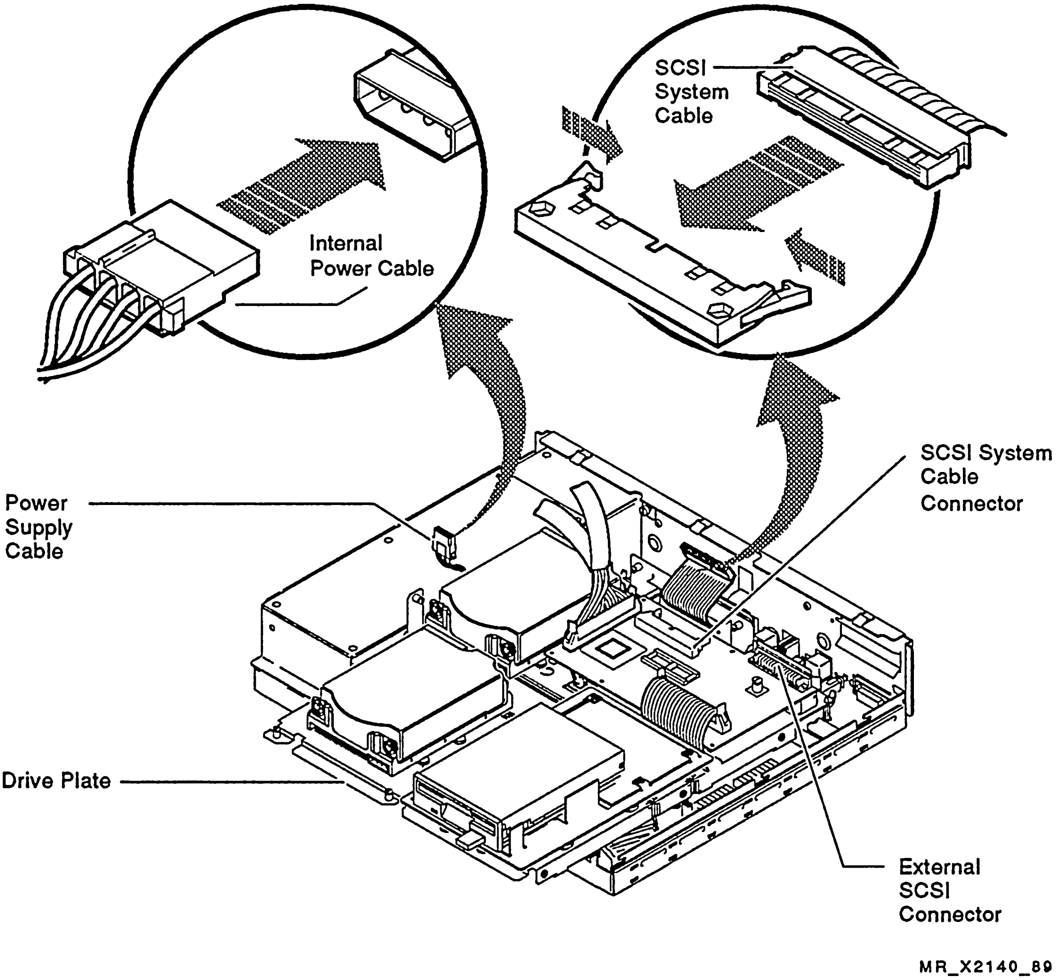

Captive Screws (2)
Captive Screws (3)
Drive Plate
Slide Mount Screws (3) with Corresponding Slide Mount Openings (3)
MR_X2139_89

2 Tighten the five captive slot-head screws on the drive plate.

3 Tighten the three slide mount cross-head screws.

4 Reconnect the system power supply cable to the male connector of the power cable (Figure 2–17).

Figure 2–17 Reconnecting Drive Plate Cables



5 Reconnect the terminator or cable to the external SCSI connector on the SCSI mass storage controller module.

6 Reconnect the SCSI system cable between the system module and the SCSI controller module. Be sure to press the connector latches completely into place.

7 Continue at Section 2.9.

2.9 Restoring the System Unit

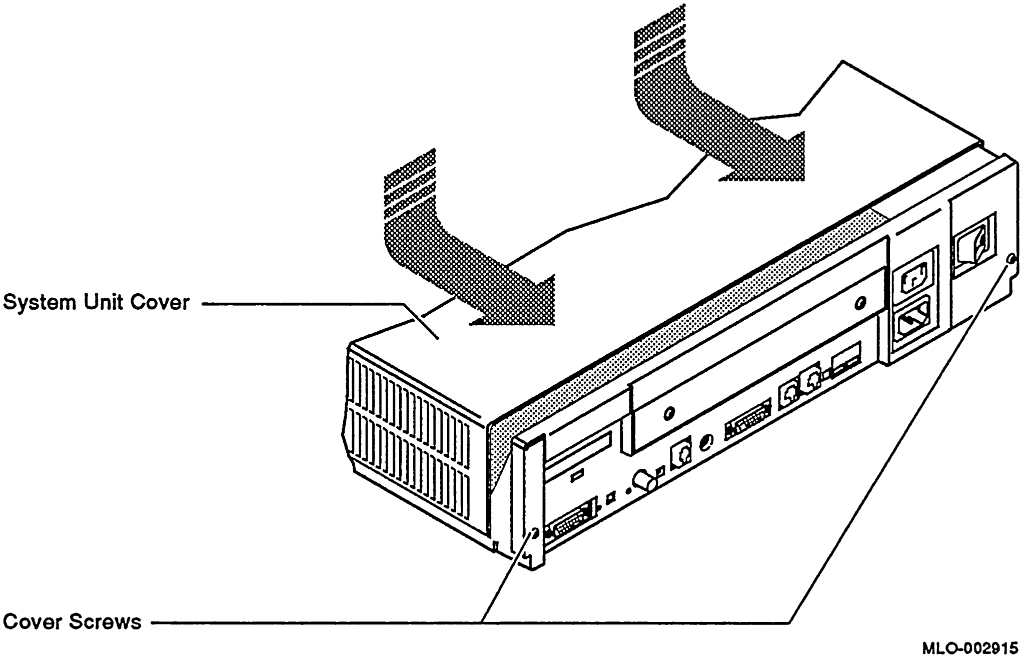
To restore the system unit:

1 Place the system cover over the system unit so that its rear opening is approximately 4 cm (1.5 in) from the rear connector panel of the system unit.

2 Make sure all internal cables are inside the system cover, and slide it toward the rear of the system unit. Tighten the two cover screws (Figure 2–18).

Warning *As with any electrical system, it is a fire hazard to turn on system power with the cover removed.*

Figure 2–18 Replacing the System Cover



The remaining steps can be performed in any sequence according to the configuration and placement of the system's components.

Warning *The monitor is heavy and you may need another person's help to lift it.*

3 Replace the monitor on top of the system unit.

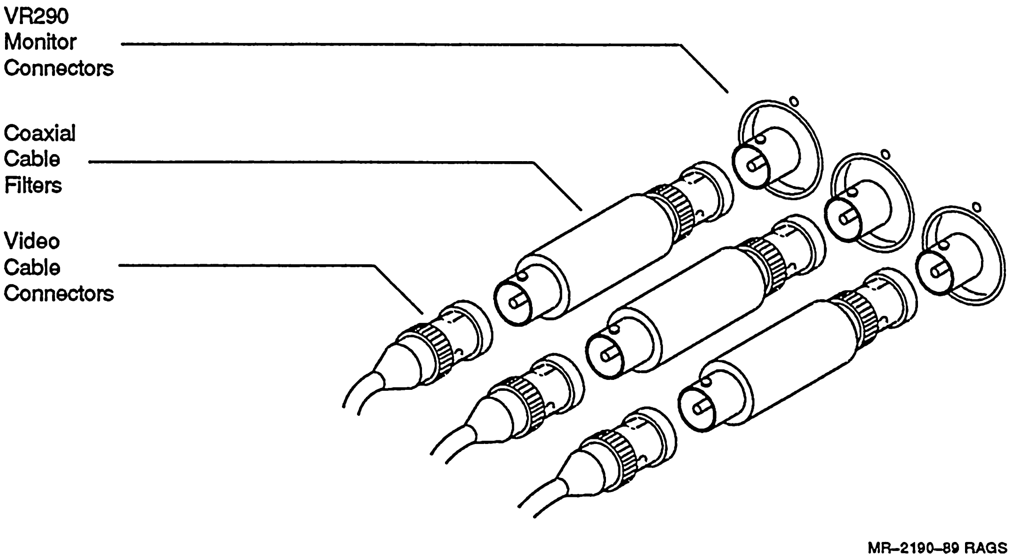
4 The correct monitor video cable is supplied with the WS01X-GA/GB graphics coprocessor installation kit. Follow the directions in the monitor guide to connect the cable to the monitor. Additionally:

- **Monochrome Monitors:** Only the green video cable is connected to a monochrome monitor; the red and blue cables are not used.
- **VR290 Monitors:** The coaxial cable filters supplied with the WS01X-GA/GB graphics coprocessor installation kit must be installed between the monitor video cable and the VR290 monitor. Install the filters as follows:

Note *Do not fasten the cable assembly to the monitor before connecting the video cables and filters.*

1 Connect the red, green, and blue video cables to the filters (Figure 2–19).

Figure 2–19 VR290 Monitor Coaxial Cable Filters



2 Connect the filters to the monitor connectors.

3 Fasten the cable assembly to the monitor.

5 Connect the following cables to the system unit:

- Keyboard cable (Figure 2–20)
- Mouse cable (Figure 2–21)
- Monitor video cable (Figure 2–22).
- ThinWire T-connector (Figure 2–23)
- Monitor power cord (Figure 2–24)

Figure 2–20 Connecting the Keyboard to the System Unit

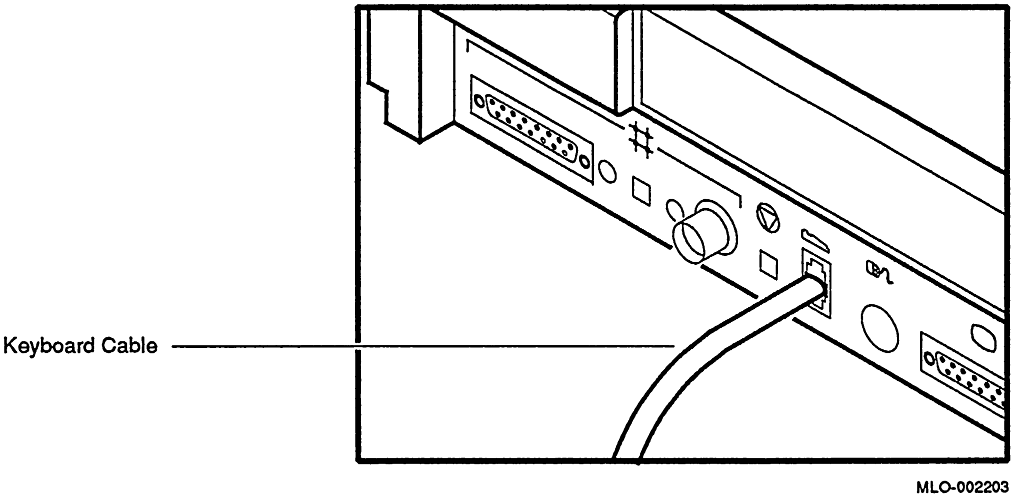


Figure 2–21 Connecting the Mouse to the System Unit

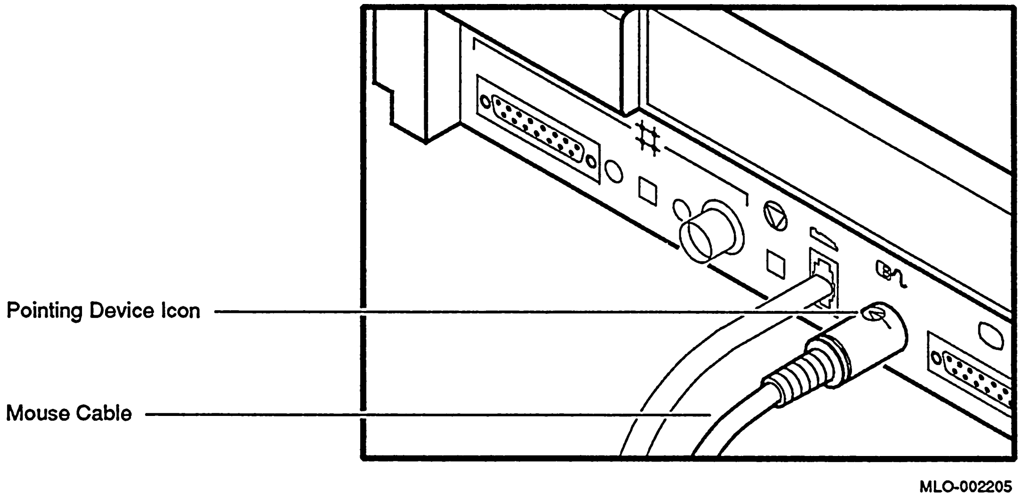


Figure 2–22 Connecting the Monitor Video Cable to the System Unit

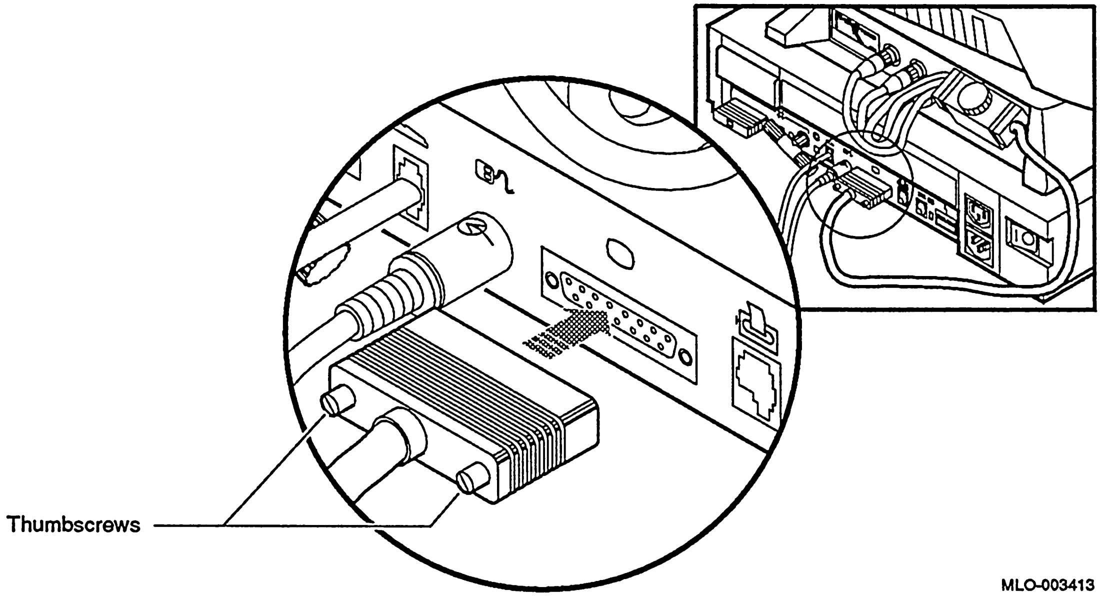
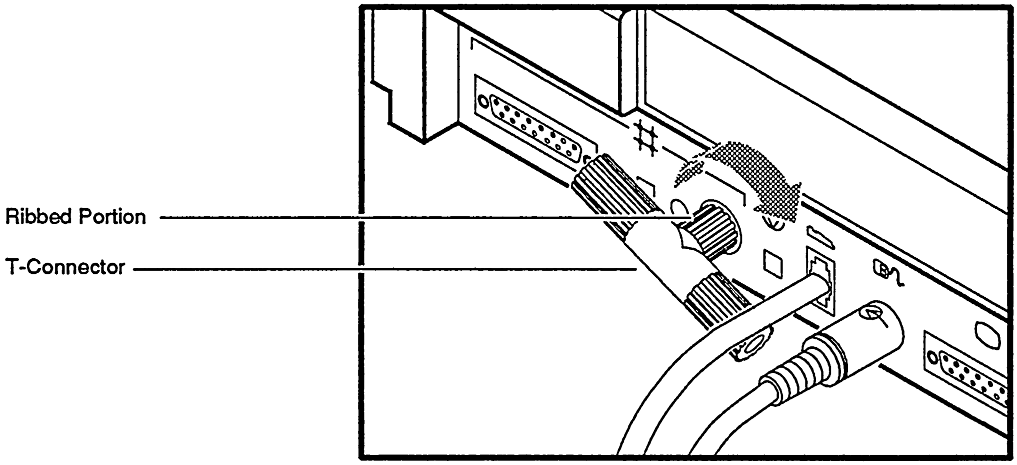
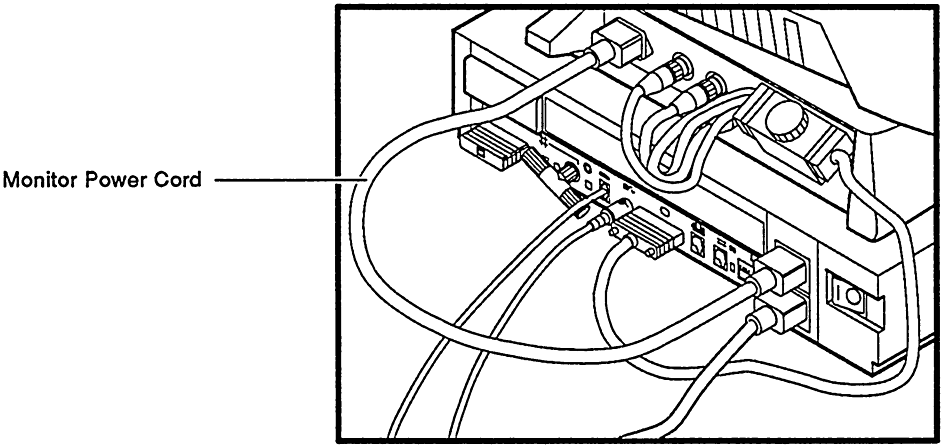


Figure 2–23 Connecting the ThinWire T-Connector to the System Unit



MLO-002209

Figure 2–24 Connecting the Monitor Power Cord to the System Unit



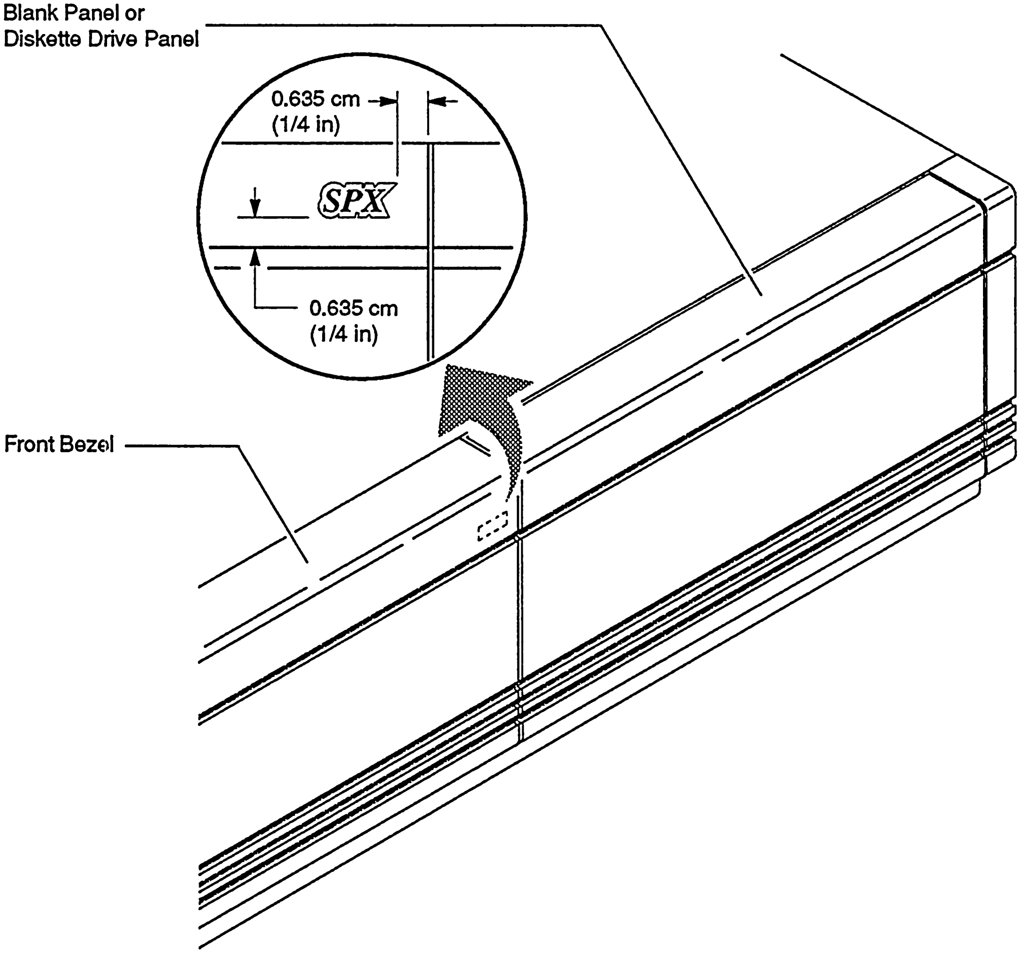
MR_X2141_89

6 Continue at Section 2.10.

2.10 Attaching the SPX Label

The installation kit includes an SPX label to identify workstations that have an installed WS01X-GA/GB graphics coprocessor. As Figure 2–25 shows, the label is installed on the front of the system unit, next to the blank panel (or diskette drive panel, if a diskette drive is installed). Install the label as follows:

Figure 2–25 SPX Label Position



- Remove the protective paper from the adhesive backing of the label.

- Press the label into position as shown in Figure 2–25.
- The WS01X-GA/GB graphics coprocessor installation is complete. Continue at Section 2.11.

2.11 Starting the System

If the system includes expansion boxes or peripheral devices (other than the monitor) that must be turned on, see the system starting procedures in the workstation owner's manual; otherwise:

1. Turn on the monitor.
2. Turn on the system unit.
3. Continue at Section 2.12 to verify the WS01X-GA/GB graphics coprocessor installation.

2.12 Testing the System

To verify that the WS01X-GA/GB graphics coprocessor is operating correctly:

1. Note any power-up error or status messages. Example 2–1 shows the types of information in the power-up display.

Example 2–1 Power-Up Display

```
KA42-B  V1.0 ❶

F...E...D...C...B...A...8...9...7_..6?..5...4...3*..2...1... ❷
   ❸                                 ❹    ❺           ❻
```

❶ The CPU name (KA42-B) and ROM version (V1.0).

❷ Test numbers for the installed system devices. Table 2–2 lists the device test numbers.

❸ Three dots (...) after the test number indicates that the device passed the power-up self-test.

❹ An underscore and two dots (_..) indicates the device is not installed or has not been tested.

❺ A question mark and two dots (?..) indicates a minor problem that probably will not interfere with normal system operation. A double question mark (??.) indicates a serious problem that will affect normal system operation.

❻ An asterisk and two dots (*..) indicates the device is installed but its ROM code has not been executed. Only device numbers 7, 6, 4, 3, or 2 can have an asterisk.

Table 2–2 Device Test Identifiers and Mnemonics

Identifier	Mnemonic	Device
F	MONO	Base video
E	CLK	System clock
D	NVR	Nonvolatile RAM
C	DZ	Serial line controller
B	MEM	Memory
A	MM	Memory controller
9	FP	Floating point unit
8	IT	Interval timer
7	SCSI-A	SCSI-A bus controller
6	SCSI-B	SCSI-B bus controller
5	SYS	Interrupt controller and Ethernet ID ROM
4	SPGFX	WS01X-GA/GB graphics coprocessor
4	8PLN	VS40X-PA graphics coprocessor
3		Reserved
2		Reserved
1	NI	Ethernet network interconnect

2 Enter the TEST 50 console command to display the system device configuration. Compare it to the information you copied from the configuration display when you prepared the system to install the WS01X-GA/GB graphics coprocessor (Section 2.1). Example 2–2 shows the types of information in the configuration display.

Example 2–2 Configuration Display

```
>>> TEST 50 Return

KA42-B  V1.0 ❶
ID 08-00-2B-07-E3-83 ❷

   MONO       0000.0001 ❸
   CLK        0000.0001
   NVR        0000.0001
   DZ         0000.0001
       00000001 00000001 00000001 00000001 00000001 000012A0 ❹
   MEM        0010.0001
        01000000        ❺
   MM         0000.0001
   FF         0000.0001
   IT         0000.0001

   SCSI-A     2828.0001   V1.30 ❻
   FFFFFF05 FFFFFF05 FFFFFF05 00000001 FFFFFF05 01000001 FFFFFF03 FFFFFF05

   SCSI-B     1C1C.0001   V1.30
   FFFFFF05 FFFFFF05 00000001 00000001 05000001 FFFFFF05 FFFFFF03 FFFFFF05

   SYS        0000.0001
   SPGFX ❼   0000.0001   V1.0
   NI         0000.0001
>>>
```

❶ The CPU name (KA42-B) and ROM version (V1.0).

❷ Ethernet hardware address

❸ Device status codes

❹ DZ status codes

❺ Code for 16 Mbytes of memory

❻ SCSI status codes

❼ WS01X-GA/GB graphics coprocessor device mnemonic. (The VS40X-PA graphics coprocessor device mnemonic is 8PLN.)

A WS01X-GA/GB graphics coprocessor status code other than 0000.0001 indicates a hard error.

For more information on the configuration display, see Chapter 3.

3 Use the TEST 0 console command to run the system exerciser and verify that the devices are interacting correctly. Example 2–3 shows the types of information displayed by the system exerciser.

Example 2–3 System Exerciser Display

```
>>> TEST 0 Return

KA42-B  V1.0          01     CU

   F  00B0   MONO    0000.0001  11 1005      0 00:00:35
   C  0080   DZ      0000.0001  14           0 00:01:12
   B  0010   MEM     0137.0001   5 00A7      0 00:02:02
   7  0090   SCSI-A  6000.0001  22 0002      0 00:02:23
                     3200.0001
   6  00A0   SCSI-B  6000.0001  15 0002      0 00:02:56
                     2200.0001
                     3200.0001
                     4100.0001
                     7200.0001
   4  00D0   SPGFX   0000.0001   9           0 00:03:55
   1  00C0   NI      0000.0001   9           0 00:04:01
   ❶   ❷      ❸        ❹        ❺               ❻

 00   0.00:08:14
?06   HLT INST
      PC - 00005A0F
>>>
```

❶ Test number column. Table 2–2 lists the device test numbers and mnemonics.

❷ Device identifier column

❸ Device mnemonic column

❹ Status or error code column

❺ Pass count column

❻ Runtime column

For more information on the system exerciser display, see Chapter 3.

4 If you have any problems, make sure that:

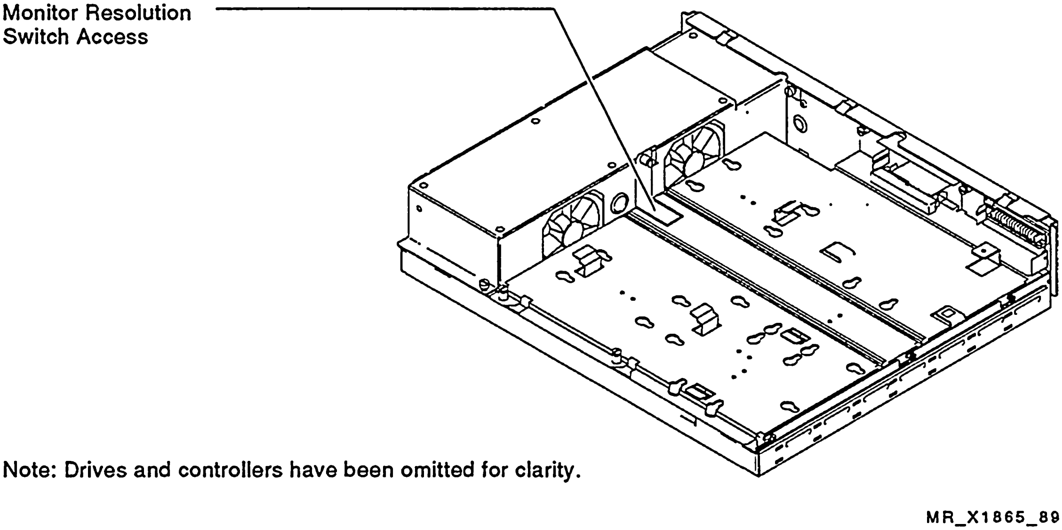
- All internal and external cables are reconnected.
- All modules are fully seated in their connectors.
- The WS01X-GA/GB graphics coprocessor resolution switch is in the correct position (Table 2–1).

2.13 Resetting the Monitor Resolution Switch

You can change the position of the monitor resolution switch after the WS01X-GA/GB graphics coprocessor is installed, but you must remove the system cover as described in Section 2.1. With the system cover removed, the monitor resolution switch is accessible through a slot in the drive plate, as shown in Figure 2–26. After you have reset the switch, replace the system cover as described in Section 2.9.

Warning *As with any electrical system, it is a fire hazard to turn on system power with the cover removed.*

Figure 2–26 Monitor Resolution Switch Access



Note: Drives and controllers have been omitted for clarity.

BLANK

3

Diagnostic Tests and Utilities

This chapter describes the WS01X-GA/GB graphics coprocessor configuration display, system exerciser diagnostic, and utilities that generate display test patterns.

3.1 Self-Test

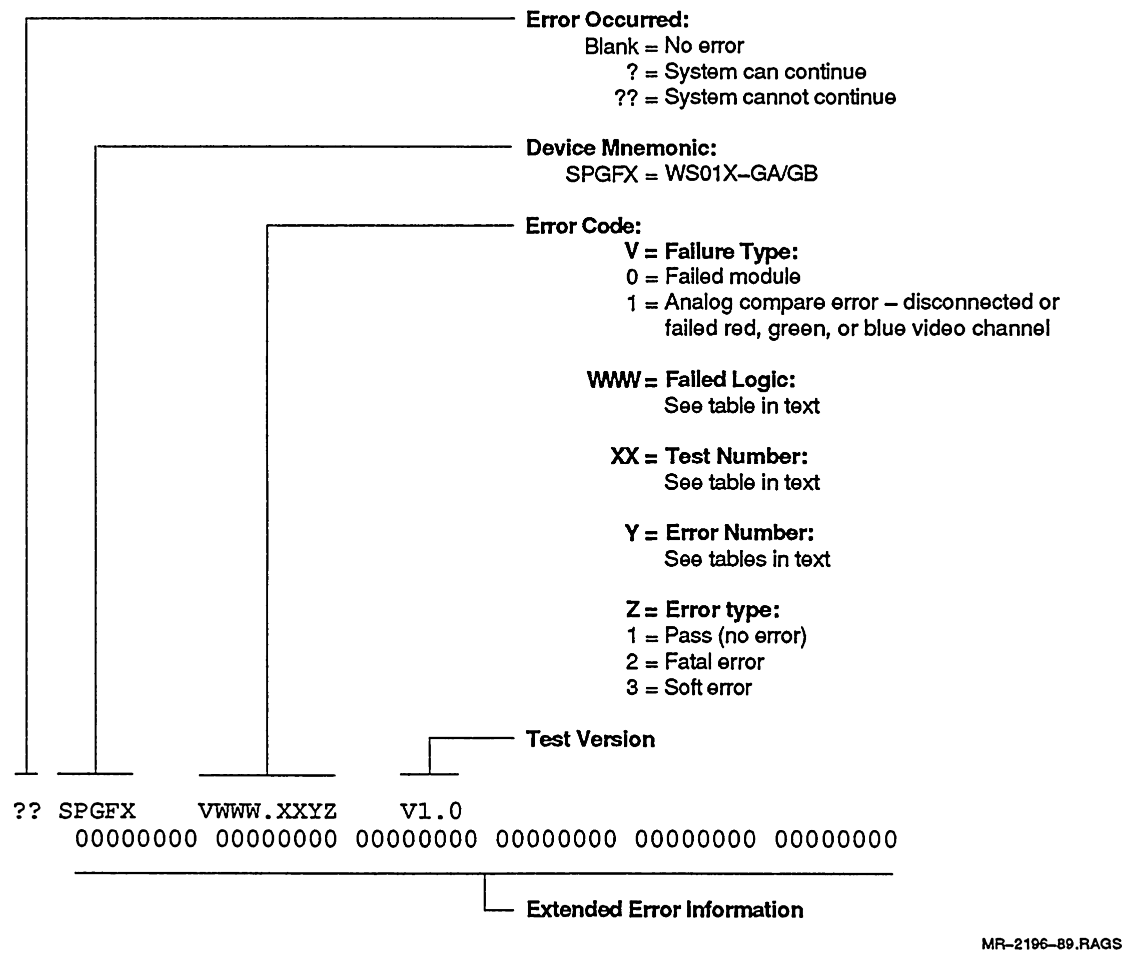
The code for the WS01X-GA/GB graphics coprocessor power-up self-tests resides in the self-test ROM on the WS01X-GA/GB graphics coprocessor module. The base system loads the code and executes it concurrently with the self-test code for other system devices. The power-up self-test (Section 2.12) provides the initial system status display.

3.2 Error Summary Display

Additional error information is provided by the error summary console command. Enter T 50 in response to the console prompt to display the error summary (also called the configuration display). Example 2–2 in Section 2.12 shows a typical system configuration display.

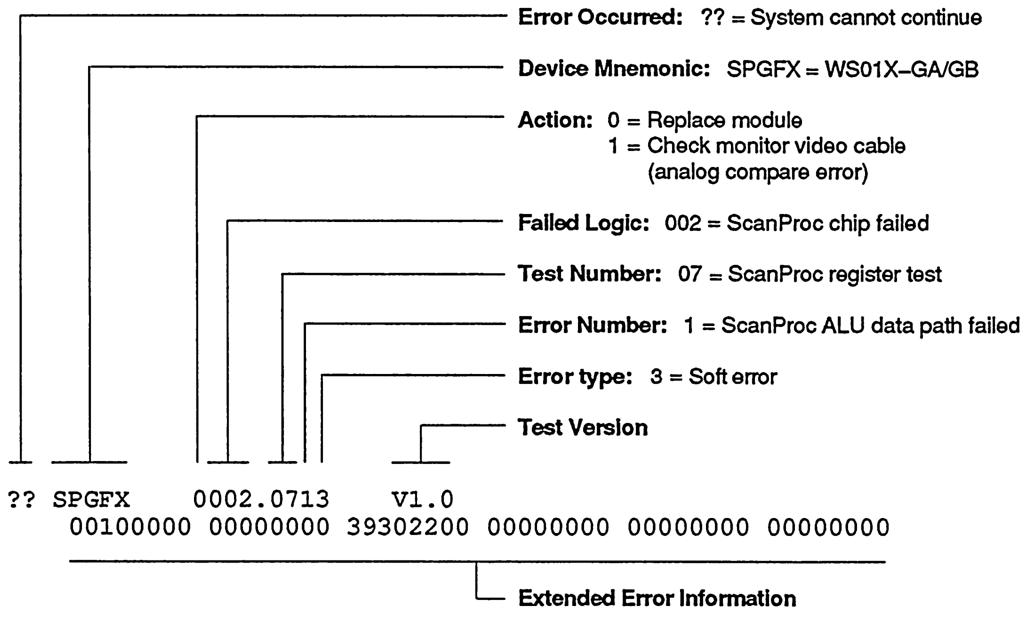
Figure 3–1 shows the format for the WS01X-GA/GB graphics coprocessor error summary. Figure 3–2 shows a hypothetical WS01X-GA/GB graphics coprocessor error summary. Table 3–1 lists the failed logic codes. Table 3–3 lists the test numbers described in Sections 3.4.1 through 3.4.33. The contents of the six 8-digit extended error information fields depend on the test number, and are also described in Sections 3.4.1 through 3.4.33. Tables 3–4 through 3–36 list the error numbers.

Figure 3–1 WS01X-GA/GB Graphics Coprocessor Error Summary Format



Note *The WS01X-GA/GB graphics coprocessor always reports a soft error (or no error) during power-up self-test so that the console output is directed to the display.*

Figure 3–2 WS01X-GA/GB Graphics Coprocessor Error Summary Display


Error Occurred: ?? = System cannot continue
Device Mnemonic: SPGFX = WS01X–GA/GB
Action: 0 = Replace module
1 = Check monitor video cable
(analog compare error)
Failed Logic: 002 = ScanProc chip failed
Test Number: 07 = ScanProc register test
Error Number: 1 = ScanProc ALU data path failed
Error type: 3 = Soft error
Test Version
Extended Error Information

```
?? SPGFX    0002.0713    V1.0
    00100000 00000000 39302200 00000000 00000000 00000000
```

Table 3–1 Failed Logic Codes

Code	Logic
001	Timing buffer chip
002	ScanProc chip
003	ScanProc0 chip
004	ScanProc1 chip
005	ScanProc2 chip
006	ScanProc3 chip
007	ScanProc4 chip
008	ScanProc5 chip
009	ScanProc6 chip
00A	ScanProc7 chip
00B	ScanProc8 chip
00C	VRAM section of the module

(continued on next page)

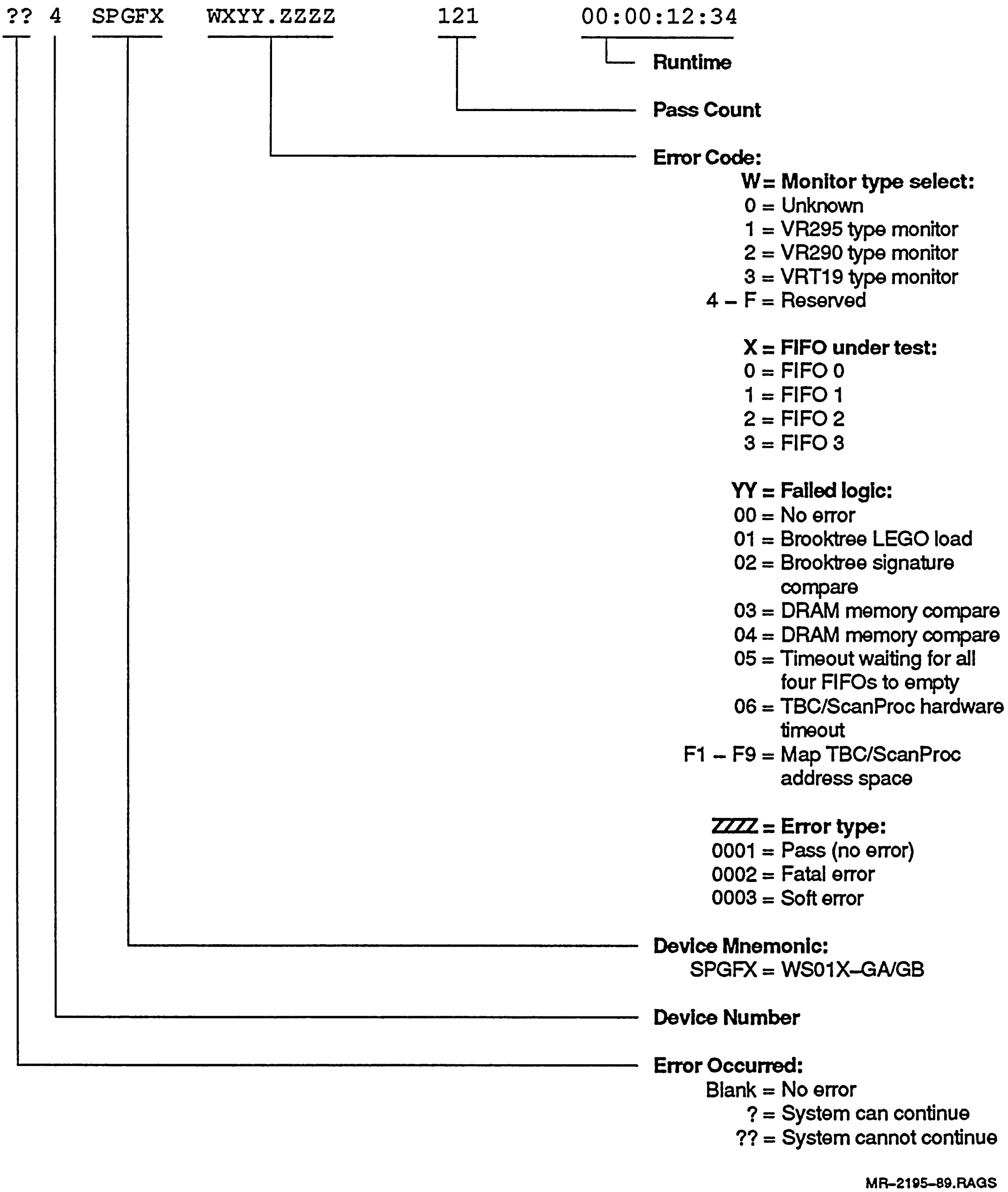
Table 3–1 (Cont.) Failed Logic Codes

Code	Logic
00D	DRAM section of the module
00E	FIFO section of the module
00F	Brooktree DAC
010–FFF	Reserved

3.3 System Exerciser Test

The code for the system exerciser also resides in the module's self-test ROM. As with self-test, the base system loads the code and executes it concurrently with the system exerciser code for other system devices. Figure 3–3 shows the fields in the WS01X-GA/GB graphics coprocessor report line of a typical system exerciser display. Note the differences in the error code field between this display and the self-test display. Table 3–2 provides more information about the system exerciser error code field.

Figure 3–3 WS01X-GA/GB Graphics Coprocessor System Exerciser Display



```
?? 4  SPGFX  WXYY.ZZZZ     121     00:00:12:34
```

Runtime

Pass Count

Error Code:

W = Monitor type select:
0 = Unknown
1 = VR295 type monitor
2 = VR290 type monitor
3 = VRT19 type monitor
4 – F = Reserved

X = FIFO under test:
0 = FIFO 0
1 = FIFO 1
2 = FIFO 2
3 = FIFO 3

YY = Failed logic:
00 = No error
01 = Brooktree LEGO load
02 = Brooktree signature compare
03 = DRAM memory compare
04 = DRAM memory compare
05 = Timeout waiting for all four FIFOs to empty
06 = TBC/ScanProc hardware timeout
F1 – F9 = Map TBC/ScanProc address space

ZZZZ = Error type:
0001 = Pass (no error)
0002 = Fatal error
0003 = Soft error

Device Mnemonic:
SPGFX = WS01X–GA/GB

Device Number

Error Occurred:
Blank = No error
? = System can continue
?? = System cannot continue

Table 3–2 decodes the system exerciser error code field.

Table 3–2 WS01X-GA/GB Graphics Coprocessor System Exerciser Error Code Field

Subfield	Value$_{16}$	Description
W		Monitor type select
	0	Unknown monitor type
	1	VR295 type monitor
	2	VR290 type monitor
	3	VRT19 type monitor
	4–F	Reserved
X		FIFO under test
	0	FIFO 0
	1	FIFO 1
	2	FIFO 2
	3	FIFO 3
YY		Failed logic
	00	No error.
	01	Brooktree LEGO load operation failed.
	02	Brooktree signature compare error.
	03	DRAM memory compare error.
	04	DRAM memory compare error.
	05	Timeout waiting for all four FIFOs to empty.
	06	TBC/ScanProc hardware timeout error.
	F1–F9	System failed to map TBC/ScanProc address space.
ZZZZ		Error type
	0001	Pass (no error)
	0002	Fatal
	0003	Soft

3.4 Test Description

Table 3–3 gives the test number and name for the tests residing in self-test ROM. The tests are described in Sections 3.4.1 through 3.4.33. The error numbers associated with the tests are listed in Tables 3–4 through 3–36. These are the error numbers that appear in the error number subfield in the error summary display (Figures 3–1 and 3–2).

Table 3–3 Test Numbers

Number_{16}	Name
01	TBC register
02	TBC horizontal timing
03	TBC vertical timing
04	TBC LEGO load
05	Brooktree register
06	Brooktree memory
07	ScanProc register
08	ScanProc scratch RAM
09	ScanProc microcode RAM
0A	FIFO direct access
0B	FIFO autoincrement location
0C	FIFO autoincrement buffer load
0D	FIFO autoincrement buffer execution
0E	Frame buffer address/data
0F	Frame buffer 4Mega pixel
10	Frame buffer write/read mask
11	ScanProc basic rectangle
12	ScanProc clipping rectangle
13	ScanProc copy rectangle
14	ScanProc fill rectangle masking
15	ScanProc draw rectangle logical OP
16	ScanProc copy rectangle logical OP
17	ScanProc copy rectangle masking
18	ScanProc copy stipple rectangle
19	ScanProc copy opaque rectangle
1A	ScanProc basic trapezoid
1B	ScanProc basic vector
1C	Frame buffer stream write
1D	Frame buffer stream read
1E	VRAM serial shift
1F	Brooktree analog compare
20	Brooktree LEGO load
21	TBC interrupt

3.4.1 TBC Register Test (01)

This test verifies the data path for each timing buffer chip (TBC) register listed in Table 3–4.

Table 3–4 TBC Register Test Errors

Error_{16}	Failed Register(s)
1	TBC control/status register (CSR)
2	TBC diagnostic register
3	TBC Cport frame buffer format register TBC Cport interrupt mask register TBC Cport interrupt status register
4	TBC GFPA frame buffer format register TBC GFPA interrupt mask register TBC GFPA interrupt status register
5	TBC FIFO threshold value register TBC FIFO semaphore register
6	TBC horizontal sync register TBC horizontal sync 2 register TBC horizontal blank register TBC vertical sync register TBC vertical blank register TBC timing control/status register (CSR) TBC table register TBC timing setup register TBC LEGO test result register
7	TBC ScanProc bus loopback register

The six 8-bit extended error information fields (Figure 3–2) are defined as follows:

Error_{16}	Field	Description
All	1	Expected data
	2	Actual data
	3	TBC address
	4–6	Undefined

3.4.2 TBC Horizontal Timing Test (02)

This test verifies the horizontal blank and sync (HBLANK, HSYNC, HSYNC2) parameters. A TBC diagnostic mode compares the nibble clock timing in the register under test to the ScanProc clock. Table 3–5 describes the errors reported by this test.

Table 3–5 TBC Horizontal Timing Test Errors

Error_{16}	Failure
1	TBC ready bit not set
2	TBC ready bit not cleared
3	TBC unknown crystal frequency
4	TBC HBLANK START not set
5	TBC HBLANK START not cleared
6	TBC HSYNC START not set
7	TBC HSYNC START not cleared
8	TBC HSYNC2 not set
9	TBC HBLANK FINISH not set
A	TBC HBLANK FINISH not cleared
B	TBC HSYNC2 FINISH not set
C	TBC HSYNC2 FINISH not cleared
D	TBC HSYNC2 not cleared

The six 8-bit extended error information fields (Figure 3–2) are defined as follows:

Error_{16}	Field	Description
1–3	1–6	Undefined.
4–D	1	Data loaded into the register under test.
	2	Data loaded into the vertical blank start register. This is required for the diagnostic mode testing.
	3–6	Undefined.

3.4.3 TBC Vertical Timing Test (03)

This test verifies the vertical blank and sync registers. Data is loaded into the register under test and checked against the number of scanlines that have transpired. Table 3–6 describes the errors reported by this test.

Table 3–6 TBC Vertical Timing Test Errors

$Error_{16}$	Failure
1	TBC CSR V0 bit. Timeout waiting for the V0 bit to toggle.
2	TBC CSR VS bit. Timeout waiting for the VS bit to toggle.
3	TBC Cport interrupt vertical blank start/vertical blank finish (VBS/VBF) bit. Failed to set the VBS and VBF bits in the Cport interrupt status register.
4	TBC vertical sync start (VSS) failure.
5	TBC vertical sync finish (VSF) failure.
6	TBC VBS failure.
7	TBC VBF failure.

The six 8-bit extended error information fields (Figure 3–2) are defined as follows:

$Error_{16}$	Field	Description
1–3	1–6	Undefined.
4–7	1	Data loaded into the register under test.
	2	Number of scanlines counted.
	3–6	Undefined.

3.4.4 TBC LEGO Load Test (04)

This test verifies the TBC control signals that are used to load the video output chip(s) from offscreen VRAM. Table 3–6 describes the errors reported by this test. Note that only the TBC can cause these errors.

Table 3–7 TBC LEGO Load Test Errors

$Error_{16}$	Failure
1	TBC failed to set the VBF bit.
2	TBC failed to set the video output chip (VOC) load bit in the timing CSR.
3	TBC failed to clear the VOC load bit in the timing CSR after a vertical retrace period.

(continued on next page)

Table 3–7 (Cont.) TBC LEGO Load Test Errors

$Error_{16}$	Failure
4	TBC failed to set the VOC load bit in the timing CSR after a vertical retrace period.
5	TBC failed continuous loading of the VOCs.

The six 8-bit extended error information fields (Figure 3–2) are defined as follows:

$Error_{16}$	Field	Description
All	1	Data loaded into timing CSR bits <0:4> before LEGO loading occurs.
	2	Data read from the timing CSR.
	3–6	Undefined.

3.4.5 Brooktree Register Test (05)

This test verifies the control signals to the Brooktree chip. Note that all the registers do not support Modulo 3 loading. Table 3–8 describes the errors reported by this test.

Table 3–8 Brooktree Register Test Errors

$Error_{16}$	Failure
1	Brooktree DAC diagnostic data path error.
2	Brooktree DAC C0 line decode error.
3	Brooktree DAC C1:C0 line decode error.
4	Brooktree DAC C1:C0 line decode error.
5	Brooktree cursor color register verify error.
6	Brooktree command/cursor/window register verify error.

The six 8-bit extended error information fields (Figure 3–2) are defined as follows:

Error_{16}	Field	Description
1	1	Expected data loaded into Brooktree register.
	2	Actual data in Brooktree register.
	3	Brooktree register under test.
	4–6	Undefined.
2	1	Actual data in Brooktree address low register.
	2	Expected data in Brooktree address low register.
	3	Actual data in Brooktree address high register.
	4	Expected data in Brooktree address high register.
	5–6	Undefined.
3–4	1–6	Undefined.
5	1	Brooktree cursor color register address.
	2	Expected RED data in upper word, actual RED data in lower word.
	3	Expected GREEN data in upper word, actual GREEN data in lower word.
	4	Expected BLUE data in upper word, actual BLUE data in lower word.
	5–6	Undefined.
6	1	Expected data loaded into Brooktree register.
	2	Actual data in Brooktree register.
	3	Brooktree register under test.
	4–6	Undefined.

3.4.6 Brooktree Memory Test (06)

This test verifies the Brooktree chip's internal address lines and all the registers that support Modulo 3 loading. Table 3–9 describes the errors reported by this test.

Table 3–9 Brooktree Memory Test Errors

Error_{16}	Failure
1	Brooktree internal address line fault.
2	Brooktree Modulo 3 addressing fault.
3	Brooktree color palette RAM failure.
4	Brooktree cursor RAM failure.

The six 8-bit extended error information fields (Figure 3–2) are defined as follows:

Error_{16}	Field	Description
1	1	Address line under test.
	2	Address line being fault-tested.
	3	Brooktree address resulting from the faulty address line(s).
	4–6	Undefined.
2	1–6	Undefined.
3	1	Brooktree cursor RAM address.
	2	Expected RED data in upper word, actual RED data in lower word.
	3	Expected GREEN data in upper word, actual GREEN data in lower word.
	4	Expected BLUE data in upper word, actual BLUE data in lower word.
	5–6	Undefined.
4	1	Brooktree cursor palette register address.
	2	Expected data in upper word, actual data in lower word.
	3–6	Undefined.

3.4.7 ScanProc Register Test (07)

This test verifies the data path to the ScanProc chip. After data path verification, the ScanProc internal ALU and MAIN bus register access are tested in every direct-access mode. Table 3–10 describes the errors reported by this test.

Table 3–10 ScanProc Register Test Errors

Error_{16}	Failure
1	ScanProc ALU0 data path failure.
2	ScanProc ALU register failure.
3	ScanProc MAIN bus register failure.
4	ScanProc host byte mask access failure.
5	ScanProc ALU register mask access failure.
6	ScanProc MAIN bus register mask access failure.
7	ScanProc ALU/MAIN mask data access failure.
8	ScanProc test output line not cleared after reset.
9	ScanProc internal diagnostic failure.

The six 8-bit extended error information fields (Figure 3–2) are defined as follows:

Error$_{16}$	Field	Description
1	1	Expected data loaded into ScanProc register.
	2	Actual data read from ScanProc register.
	3	ScanProc 0 ALU0 register address.
	4–6	Undefined.
2–3	1	Expected data loaded into ScanProc register.
	2	Actual data read from ScanProc register.
	3	ScanProc register address.
	4	ScanProc number under test.
	5–6	Undefined.
4–7	1	Expected data loaded into ScanProc register.
	2	Actual data read from ScanProc register.
	3	ScanProc register address.
	4	Byte mask lines in least significant nibble.
	5	ScanProc number under test.
	6	Undefined.
8–9	1	Expected data in the TBC ROM/configuration register.
	2	Actual data in the TBC ROM/configuration register.
	3	TBC ROM/configuration register address.
	4–6	Undefined.

3.4.8 ScanProc Scratch RAM Test (08)

This test verifies the ScanProc scratch RAM data and mask bits, and is executed on all ScanProcs in the system. The first part of the test verifies the internal address lines to the scratch RAM, and the remainder verifies the scratch RAM internal data cells and mask data. Table 3–11 describes the errors reported by this test.

Table 3–11 ScanProc Scratch RAM Test Errors

Error$_{16}$	Failure
1	ScanProc scratch RAM addressing failure.
2	ScanProc scratch RAM data failure.
3	ScanProc scratch RAM mask data failure.

The six 8-bit extended error information fields (Figure 3–2) are defined as follows:

$Error_{16}$	Field	Description
1	1	First address line under test.
	2	Second address line under test.
	3	Resulting ScanProc scratch RAM address error.
	4	ScanProc number under test.
	5–6	Undefined.
2–3	1	Expected data loaded into scratch RAM.
	2	Actual data read from scratch RAM.
	3	Internal scratch RAM address (range: 0–79).
	4	ScanProc number under test.
	5–6	Undefined.

3.4.9 ScanProc Microcode RAM Test (09)

This test verifies the internal address lines and integrity of the ScanProc internal microcode RAM. Table 3–12 describes the errors reported by this test.

Table 3–12 ScanProc Microcode RAM Test Errors

$Error_{16}$	Failure
1	Addressing error in microcode RAM low field.
2	Addressing error in microcode RAM high field.
3	Data error in microcode RAM low field.
4	Data error in microcode RAM high field.

The six 8-bit extended error information fields (Figure 3–2) are defined as follows:

$Error_{16}$	Field	Description
1–2	1	Expected data in microcode RAM.
	2	Actual data in microcode RAM.
	3	Internal microcode RAM location address.
	4	First address line under test.
	5	Second address line under test.
	6	Undefined.
3–4	1	Expected data in microcode RAM.
	2	Actual data in microcode RAM.
	3	Internal microcode RAM location address.
	4–6	Undefined.

3.4.10 FIFO Direct Access Test (0A)

This test performs a data path test, address line test, and cell verification test on the four FIFOs to verify direct access to the FIFO RAM. Table 3–13 describes the errors reported by this test.

Table 3–13 FIFO Direct Access Test Errors

Error_{16}	Failure
1	FIFO direct mode access data path error.
2	FIFO direct mode access address path error.
3	FIFO direct mode access memory error.

The six 8-bit extended error information fields (Figure 3–2) are defined as follows:

Error_{16}	Field	Description
1 and 3	1	Expected data in FIFO RAM.
	2	Actual data in FIFO RAM.
	3	FIFO address location of failure.
	4–6	Undefined.
2	1	First FIFO address line under test.
	2	Second FIFO address line under test.
	3	FIFO address equal to the logical-OR of the two address lines.
	4–6	Undefined.

3.4.11 FIFO Autoincrement Location Test (0B)

The TBC autoincrement function loads data into the FIFO and updates the TBC GET, PUT, and POINT counters. This test verifies the TBC and FIFO functions listed in Table 3–14.

Table 3–14 FIFO Autoincrement Location Test Errors

Error_{16}	Failure
1	FIFO PUT register not initialized to zero.
2	FIFO GET register not initialized to zero.
3	FIFO COUNT register not initialized to correct value.

(continued on next page)

Table 3–14 (Cont.) FIFO Autoincrement Location Test Errors

Error_{16}	Failure
4	FIFO PUT register has incorrect value.
5	FIFO GET register has incorrect value.
6	FIFO COUNT register has incorrect value.
7	FIFO location was not updated correctly in autoincrement mode.
8	FIFO location should not have been updated in autoincrement mode.
9	FIFO autoincrement read value is incorrect.
A	FIFO PUT register has incorrect value from read.
B	FIFO GET register has incorrect value from read.
C	FIFO COUNT register has incorrect value from read.

The six 8-bit extended error information fields (Figure 3–2) are defined as follows:

Error_{16}	Field	Description
All	1	Expected register data.
	2	Actual register data.
	3	Address of register under test.
	4–6	Undefined.

3.4.12 FIFO Autoincrement Buffer Load Test (0C)

This test verifies the FIFO autoincrement buffers for each FIFO. Data is written to the autoincrement buffer range and stored data is verified by direct access. The TBC GET, PUT, and COUNT registers are checked for correct updates. Table 3–15 describes the errors reported by this test.

Table 3–15 FIFO Autoincrement Buffer Load Test Errors

Error_{16}	Failure
1	FIFO has incorrect data after autoincrement buffer write address strobe.
2	FIFO has incorrect data after autoincrement buffer write data strobe.

(continued on next page)

Table 3–15 (Cont.) FIFO Autoincrement Buffer Load Test Errors

$Error_{16}$	Failure
3	FIFO PUT register has incorrect value.
4	FIFO GET register has incorrect value.
5	FIFO COUNT register has incorrect value.
6	FIFO PUT register has incorrect value.
7	FIFO GET register has incorrect value.
8	FIFO COUNT register has incorrect value.
9	FIFO has incorrect data after autoincrement buffer write address strobe.
A	FIFO has incorrect data after autoincrement buffer write data strobe.
B	FIFO PUT register has incorrect value after FIFO enable.
C	FIFO GET register has incorrect value after FIFO enable.
D	FIFO transfer wrote incorrect data.

The six 8-bit extended error information fields (Figure 3–2) are defined as follows:

$Error_{16}$	Field	Description
All	1	Expected register data.
	2	Actual register data.
	3	Address of register under test.
	4–6	Undefined.

3.4.13 FIFO Autoincrement Buffer Execution Test (0D)

This is a more extensive autoincrement buffers test than test 0C. A FIFO is loaded with data, enabled, and the data is transferred to another FIFO and verified. The test is performed on all FIFOs. Table 3–16 describes the errors reported by this test.

Table 3–16 FIFO Autoincrement Buffer Execution Test Errors

$Error_{16}$	Failure
1	FIFO 0 timeout error—FIFO never emptied.
2	FIFO 0 data transfer failed.

(continued on next page)

Table 3–16 (Cont.) FIFO Autoincrement Buffer Execution Test Errors

Error_{16}	Failure
3	FIFO 1 timeout error—FIFO never emptied.
4	FIFO 1 data transfer failed.
5	FIFO 2 timeout error—FIFO never emptied.
6	FIFO 2 data transfer failed.
7	FIFO 3 timeout error—FIFO never emptied.
8	FIFO 3 data transfer failed.

The six 8-bit extended error information fields (Figure 3–2) are defined as follows:

Error_{16}	Field	Description
1, 3, 5, 7	1	Expected FIFO COUNT register data.
	2	Actual FIFO COUNT register data after timeout.
	3	FIFO COUNT register address.
	4–6	Undefined.
2, 4, 6, 8	1	Expected destination FIFO data.
	2	Actual destination FIFO data.
	3	Destination FIFO error address.
	4–6	Undefined.

3.4.14 Frame Buffer Address/Data Test (0E)

This test verifies the data path to the VRAM and DRAM and detects address line shorts or opens. Table 3–17 describes the errors reported by this test.

Table 3–17 Frame Buffer Address/Data Test Errors

Error_{16}	Failure
1	Frame buffer VRAM data path failure.
2	Frame buffer DRAM data path failure.
3	Frame buffer VRAM/DRAM data failure.
4	Frame buffer VRAM/DRAM address line failure.

The six 8-bit extended error information fields (Figure 3–2) are defined as follows:

Error$_{16}$	Field	Description
1–3	1	Expected VRAM/DRAM data.
	2	Actual VRAM/DRAM data.
	3	Address of failed VRAM/DRAM location.
	4–6	Undefined.
4	1	First address line under test.
	2	Second address line under test.
	3	Resulting erroneous VRAM/DRAM address with first and second address lines set.
	4–6	Undefined.

3.4.15 Frame Buffer 4Mega Pixel Test (0F)

This test verifies every VRAM and DRAM cell. Table 3–18 describes the errors reported by this test.

Table 3–18 Frame Buffer 4Mega Pixel Test Errors

Error$_{16}$	Failure
1	Refresh error detected at ScanProc.
2	Frame buffer VRAM/DRAM cell verification error.

The six 8-bit extended error information fields (Figure 3–2) are defined as follows:

Error$_{16}$	Field	Description
All	1	Expected VRAM/DRAM data.
	2	Actual VRAM/DRAM data.
	3	Address of failed VRAM/DRAM location.
	4–6	Undefined.

3.4.16 Frame Buffer Write/Read Mask Test (10)

This test verifies the VRAM/DRAM write-per-bit function. Table 3–19 describes the errors reported by this test.

Table 3–19 Frame Buffer Write/Read Mask Test Errors

Error_{16}	Failure
1	Frame buffer write-mask failure using FB_MASK[0].
2	Frame buffer write-mask failure using FB_MASK[1].
3	Frame buffer read-mask failure using FB_MASK[0].
4	Frame buffer read-mask failure using FB_MASK[1].

The six 8-bit extended error information fields (Figure 3–2) are defined as follows:

Error_{16}	Field	Description
All	1	Expected VRAM/DRAM data.
	2	Actual VRAM/DRAM data.
	3	Address of failed VRAM/DRAM location.
	4	Frame buffer mask data.
	5–6	Undefined.

3.4.17 ScanProc Basic Rectangle Test (11)

This test verifies ScanProc's ability to draw a 16 × 16 rectangle in all drawing directions. The resulting rectangle is verified in video memory through direct access into the frame buffer. Table 3–20 describes the errors reported by this test.

Table 3–20 ScanProc Basic Rectangle Test Errors

Error_{16}	Failure
1	ScanProc timed out drawing the rectangle.
2	Rectangle incorrectly drawn in frame buffer.

The six 8-bit extended error information fields (Figure 3–2) are defined as follows:

Error_{16}	Field	Description
1	1–6	Undefined.

Error$_{16}$	Field	Description
2	1	Expected frame buffer data.
	2	Actual frame buffer data.
	3	Frame buffer address of failure.
	4	Pixel depth for Cport frame buffer format register.
	5	Test case number.
	6	Undefined.

3.4.18 ScanProc Clipping Rectangle Test (12)

This test verifies the ScanProc's ability to draw an object using a clipping rectangle. The resulting rectangle is verified in video memory through direct access into the frame buffer. Table 3–21 describes the errors reported by this test.

Table 3–21 ScanProc Clipping Rectangle Test Errors

Error$_{16}$	Failure
1	ScanProc timed out drawing the rectangle.
2	Rectangle incorrectly drawn in frame buffer using a clipping rectangle.

The six 8-bit extended error information fields (Figure 3–2) are defined as follows:

Error$_{16}$	Field	Description
1	1–6	Undefined.
2	1	Expected frame buffer data.
	2	Actual frame buffer data.
	3	Frame buffer address of failure.
	4	Pixel depth for Cport frame buffer format register.
	5	Test case number.
	6	Undefined.

3.4.19 ScanProc Copy Rectangle Test (13)

This test verifies the ScanProc's ability to copy a rectangle from one frame buffer location to another. The resulting rectangle is verified in video memory through direct access into the frame buffer. Table 3–22 describes the errors reported by this test.

Table 3–22 ScanProc Copy Rectangle Test Errors

$Error_{16}$	Failure
1	ScanProc timed out drawing the rectangle.
2	Rectangle copied incorrectly in frame buffer.

The six 8-bit extended error information fields (Figure 3–2) are defined as follows:

$Error_{16}$	Field	Description
1	1–6	Undefined.
2	1	Expected frame buffer data.
	2	Actual frame buffer data.
	3	Frame buffer address of failure.
	4	Pixel depth for Cport frame buffer format register.
	5	Test case number.
	6	Undefined.

3.4.20 ScanProc Fill Rectangle Masking Test (14)

This test verifies the ScanProc's ability to draw a rectangle using the plane masking operation. The resulting rectangle is verified in video memory through direct access into the frame buffer. Table 3–23 describes the errors reported by this test.

Table 3–23 ScanProc Fill Rectangle Masking Test Errors

$Error_{16}$	Failure
1	Rectangle incorrectly drawn in frame buffer with write masking.
2	Rectangle incorrectly drawn in frame buffer with read masking.

The six 8-bit extended error information fields (Figure 3–2) are defined as follows:

Error_{16}	Field	Description
All	1	Expected frame buffer data.
	2	Actual frame buffer data.
	3	Frame buffer address of failure.
	4–6	Undefined.

3.4.21 ScanProc Draw Rectangle Logical OP Test (15)

This test verifies the ScanProc's ability to draw a rectangle using all 16 logical operations. The resulting rectangle is verified in video memory through direct access into the frame buffer. Table 3–24 describes the errors reported by this test.

Table 3–24 ScanProc Draw Rectangle Logical OP Test Errors

Error_{16}	Failure
1	Detected illegal pixel depth for TBC Cport format register.
2	ScanProc failed to complete the drawing operation.
3	Failed to draw rectangle with specified logical operation.
4	Draw rectangle out-of-bounds failure.

The six 8-bit extended error information fields (Figure 3–2) are defined as follows:

Error_{16}	Field	Description
1–2	1–6	Undefined.
3–4	1	Expected frame buffer data.
	2	Actual frame buffer data.
	3	Frame buffer address of failure.
	4	Pixel depth for Cport frame buffer format register.
	5	Logical operation under test.
	6	Undefined.

3.4.22 ScanProc Copy Rectangle Logical OP Test (16)

This test verifies the ScanProc's ability to copy a rectangle using all 16 logical operations. The resulting rectangle is verified in video memory through direct access into the frame buffer. Table 3–25 describes the errors reported by this test.

Table 3–25 ScanProc Copy Rectangle Logical OP Test Errors

Error_{16}	Failure
1	ScanProc failed to complete the rectangle drawing operation.
2	ScanProc failed to complete the rectangle drawing operation.
3	ScanProc failed to complete the rectangle copy operation.
4	Failed to copy rectangle with specified logical operation.

The six 8-bit extended error information fields (Figure 3–2) are defined as follows:

Error_{16}	Field	Description
1–3	1–6	Undefined.
4	1	Expected frame buffer data.
	2	Actual frame buffer data.
	3	Frame buffer address of failure.
	4	Pixel depth for Cport frame buffer format register.
	5	Logical operation under test.
	6	Undefined.

3.4.23 ScanProc Copy Rectangle Masking Test (17)

This test verifies the ScanProc's ability to copy a rectangle using the plane masking operation. The resulting rectangle is verified in video memory through direct access into the frame buffer. Table 3–26 describes the errors reported by this test.

Table 3–26 ScanProc Copy Rectangle Masking Test Errors

Error_{16}	Failure
1	Rectangle incorrectly copied in frame buffer with write masking.
2	Rectangle incorrectly copied in frame buffer with read masking.
3	Timeout copying the rectangle with masking.

The six 8-bit extended error information fields (Figure 3–2) are defined as follows:

$Error_{16}$	Field	Description
1–2	1	Expected frame buffer data.
	2	Actual frame buffer data.
	3	Frame buffer address of failure.
	4–6	Undefined.
3	1–6	Undefined

3.4.24 ScanProc Copy Stipple Rectangle Test (18)

This test verifies the ScanProc's ability to copy a stipple rectangle from one frame buffer location to another. The resulting rectangle is verified in video memory through direct access into the frame buffer. Table 3–27 describes the errors reported by this test.

Table 3–27 ScanProc Copy Stipple Rectangle Test Errors

$Error_{16}$	Failure
1	ScanProc timed out drawing the rectangle.
2	Stipple rectangle copied incorrectly in frame buffer.
3	Stipple rectangle copied incorrectly in frame buffer.

The six 8-bit extended error information fields (Figure 3–2) are defined as follows:

$Error_{16}$	Field	Description
1	1–6	Undefined.
2–3	1	Expected frame buffer data.
	2	Actual frame buffer data.
	3	Frame buffer address of failure.
	4	Pixel depth for Cport frame buffer format register.
	5–6	Undefined.

3.4.25 ScanProc Copy Opaque Rectangle Test (19)

This test verifies the ScanProc's ability to copy an opaque rectangle from one frame buffer location to another. The resulting rectangle is verified in video memory through direct access into the frame buffer. Table 3–28 describes the errors reported by this test.

Table 3–28 ScanProc Copy Opaque Rectangle Test Errors

$Error_{16}$	Failure
1	ScanProc timed out drawing the rectangle.
2	Opaque rectangle copied incorrectly in frame buffer.
3	Opaque rectangle copied incorrectly in frame buffer.

The six 8-bit extended error information fields (Figure 3–2) are defined as follows:

$Error_{16}$	Field	Description
1	1–6	Undefined.
2–3	1	Expected frame buffer data.
	2	Actual frame buffer data.
	3	Frame buffer address of failure.
	4	Pixel depth for Cport frame buffer format register.
	5–6	Undefined.

3.4.26 ScanProc Basic Trapezoid Test (1A)

This test verifies ScanProc's ability to draw a trapezoid in frame buffer memory. The resulting trapezoid is verified in video memory through direct access into the frame buffer. Table 3–29 describes the errors reported by this test.

Table 3–29 ScanProc Basic Trapezoid Test Errors

$Error_{16}$	Failure
1	Trapezoid timeout error occurred.
2	Trapezoid incorrectly drawn in frame buffer.

The six 8-bit extended error information fields (Figure 3–2) are defined as follows:

$Error_{16}$	Field	Description
1	1–6	Undefined.

Error_{16}	Field	Description
2	1	Expected frame buffer data.
	2	Actual frame buffer data.
	3	Frame buffer address of failure.
	4	Trapezoid case under test.
	5–6	Undefined.

3.4.27 ScanProc Basic Vector Test (1B)

This test verifies ScanProc's ability to draw a vector in frame buffer memory. The resulting vector is verified in video memory through direct access into the frame buffer. Table 3–30 describes the errors reported by this test.

Table 3–30 ScanProc Basic Vector Test Errors

Error_{16}	Failure
1	Vector timeout error occurred.
2	Vector incorrectly drawn in frame buffer.

The six 8-bit extended error information fields (Figure 3–2) are defined as follows:

Error_{16}	Field	Description
1	1–6	Undefined.
2	1	Expected frame buffer data.
	2	Actual frame buffer data.
	3	Frame buffer address of failure.
	4	Vector case under test.
	5–6	Undefined.

3.4.28 Frame Buffer Stream-Write Test (1C)

This test verifies a frame buffer stream-write operation. Data is loaded into the FIFO under test and a stream transfer operation is started. When the transfer is complete, data is verified in the frame buffer. Table 3–31 describes the errors reported by this test.

Table 3–31 Frame Buffer Stream-Write Test Errors

Error_{16}	Failure
1	Timeout waiting for the streaming transfer to finish.
2	Stream write failed—incorrect data in frame buffer.

The six 8-bit extended error information fields (Figure 3–2) are defined as follows:

Error_{16}	Field	Description
1	1	FIFO under test.
	2–6	Undefined.
2	1	Expected frame buffer data.
	2	Actual frame buffer data.
	3	Frame buffer address of failure.
	4	FIFO under test.
	5–6	Undefined.

3.4.29 Frame Buffer Stream-Read Test (1D)

This test verifies a frame buffer stream-read operation. Data is loaded into the FIFO under test and a stream transfer operation is started. When the transfer is complete, data is verified in the frame buffer. Table 3–32 describes the errors reported by this test.

Table 3–32 Frame Buffer Stream-Read Test Errors

Error_{16}	Failure
1	Timeout waiting for the streaming transfer to finish.
2	Stream read failed—incorrect data in FIFO.

The six 8-bit extended error information fields (Figure 3–2) are defined as follows:

Error_{16}	Field	Description
1	1	FIFO under test.
	2–6	Undefined.

Error_{16}	Field	Description
2	1	Expected FIFO data.
	2	Actual FIFO data.
	3	FIFO under test.
	4–6	Undefined.

3.4.30 VRAM Serial Shift Test (1E)

This test verifies the VRAM serial-shifting function, data multiplexing, and data input to the Brooktree DAC. The frame buffer is initialized with a pattern that tests for any shorts or opens on the DAC input. The DAC signature is compared to an expected value. Table 3–33 describes the errors reported by this test.

Table 3–33 VRAM Serial Shift Test Errors

Error_{16}	Failure
1	Signature failure on Brooktree pixel A inputs.
2	Signature failure on Brooktree pixel B inputs.
3	Signature failure on Brooktree pixel C inputs.
4	Signature failure on Brooktree pixel D inputs.

The six 8-bit extended error information fields (Figure 3–2) are defined as follows:

Error_{16}	Field	Description
All	1	Expected DAC signature.
	2	Actual DAC signature.
	3–6	Undefined.

3.4.31 Brooktree Analog Compare Test (1F)

This test verifies the analog outputs of the Brooktree DAC. Table 3–34 describes the errors reported by this test.

Table 3–34 Brooktree Analog Compare Test Errors

Error_{16}	Failure
1	RED analog output compare to 145 mV reference error.
2	RED greater than 145 mV analog compare error.
3	GREEN greater than 145 mV analog compare error.
4	RED less than BLUE analog compare error.
5	RED greater than BLUE analog compare error.
6	GREEN less than BLUE analog compare error.
7	GREEN greater than BLUE analog compare error.

The six 8-bit extended error information fields (Figure 3–2) are defined as follows:

Error_{16}	Field	Description
All	1	Expected DAC test register.
	2	Actual DAC test register first compare.
	3	Actual DAC test register second compare.
	4–6	Undefined.

3.4.32 Brooktree LEGO Load Test (20)

This test verifies the ability to load the Brooktree chip from offscreen VRAM using the TBC's LEGO load operation. This tests the VRAM serial-shift logic to the DAC. Loaded data is then verified in the Brooktree register. Table 3–35 describes the errors reported by this test.

Table 3–35 Brooktree LEGO Load Test Errors

Error_{16}	Failure
1	Illegal pixel depth for TBC Cport format register.
2	Illegal pixel depth for TBC Cport format register.
3	TBC failed to load the Brooktree chip.
4	Brooktree register compare error.
5	Brooktree register compare error.

The six 8-bit extended error information fields (Figure 3–2) are defined as follows:

Error_{16}	Field	Description
1–3	1–6	Undefined.
4	1	Brooktree register address.
	2	Expected data.
	3	Actual data.
	4–6	Undefined.
5	1	Brooktree color palette address.
	2	Expected data in color palette RGB.
	3	Actual data in color palette RED data.
	4	Actual data in color palette GREEN data.
	5	Actual data in color palette BLUE data.
	6	Actual test register from Brooktree DAC second compare.

3.4.33 TBC Interrupt Test (21)

This test verifies two interrupt vectors for the module. The first vector is generated by the TBC Cport interrupt register, and the second is generated by the TBC/ScanProc reset hardware. Table 3–36 describes the errors reported by this test.

Table 3–36 TBC Interrupt Test Errors

Error_{16}	Failure
1	Cport status register data is incorrect.
2	Hardware timeout failed to trigger.
3	Failed to clear the timeout bit in the TBC diagnostic ROM/configuration register.
4	Timeout waiting for TBC/ScanProc reset.

The six 8-bit extended error information fields (Figure 3–2) are defined as follows:

Error_{16}	Field	Description
1 and 4	1–6	Undefined.
2 and 3	1	Expected register data.
	2	Actual register data.
	3	Register address.
	4–6	Undefined.

3.5 Monitor Test Pattern Utilities

The WS01X-GA/GB graphics coprocessor provides display test patterns for visually verifying video output and display quality. Table 3–37 lists the console commands and and describes the associated test pattern.

Table 3–37 Display Test Patterns

Console Command	Test Pattern
T 80	Monitor alignment pattern. Displays a circle in the center of the screen and squares with a dot in the center of each square.
T 81	Es. The screen is filled with E characters.
T 82	White screen.
T 83	Four vertical color bars.
T 84	Red screen.
T 85	Green screen.
T 86	Blue screen.
T 87	Eight vertical color bars.
T 88	Eight vertical gray scale bars.
T 89	Scrolling Hs. The screen is filled with H characters that scroll upwards. This pattern is designed to run without end and can only be terminated by resetting the system.

BLANK

A

Part Numbers

Table A–1 lists the part numbers applicable to the WS01X-GA/GB graphics coprocessor.

Table A–1 WS01X-GA/GB Graphics Coprocessor Part Numbers

Part Number	Description
54-19623-01	WS01X-GA/GB graphics coprocessor module
EK-WS01X-OS	WS01X-GA/GB Graphics Coprocessor Owner's Manual
MP-02998-01	WS01X maintenance print set
74-40894-01	Module mounting bracket A
74-40895-01	Module mounting bracket B
74-40896-01	Module mounting bracket C
90-09984-07	Module mounting bracket screws
17-01992-01	Monitor video cable
12-33126-01	VR290 monitor coaxial cable filter
74-40937-01	SPX label

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